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Electrical Contacts on (111)A GaAs.

David Lovell

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ATR光電波通信研究所

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Name: David R. Lovell

Dept: Optical and Electronic Devices

Research Theme: Electrical Contacts on (111)A GaAs.

Period of Stay: 18 months from Feb. 1991 to July 1992.

Summary of Results:

1. Low resistance Ni/AuGe/Au contacts have been demonstrated on Si-doped n-type (111)A epitaxial GaAs.
2. Differences in the surface chemistry of n-type MBE epi-layers grown on (111)A and (100) GaAs have no affect on the contact resistance of Ni/AuGe/Au ohmic contacts.
3. Low resistance Mn/Au ohmic contacts have been demonstrated on Si doped p-type (111)A epitaxial GaAs.
4. Differences in the surface chemistry between (111)A GaAs and (100) GaAs affect the properties of Schottky contacts on these surfaces.
5. The surface state density of (111)A GaAs is lower than the surface state density of (100) GaAs.
6. The general relation $E_g = \phi_{Bn} + \phi_{Bp}$ applies to (111)A GaAs.

Activities:

Investigate Ohmic Contacts on (111)A GaAs.

Investigate Schottky Contacts on (111)A GaAs.

Investigate Field Effect Transistors on (111)A GaAs.

Papers.

Titanium/Gold Schottky Contacts on P-Type GaAs grown on (111)A and (100) GaAs Substrates Using Molecular Beam Epitaxy.
D.R. Lovell, T. Yamamoto, M. Inai, T. Takebe and K. Kobayashi:
Jpn. J. Appl. Phys. Part 2, Vol. 31, No. 7B, pp. L924-L927. July 15, 1992.

Estimation of the Surface State Density of N-Type (111)A GaAs Grown Using Molecular Beam Epitaxy.
D.R. Lovell, T. Takebe, T. Yamamoto, M. Inai, K. Kobayashi and
T. Watanabe: To be submitted to JJAP.

Equivalent Ni/AuGe/Au Ohmic Contacts on N-Type (111)A and (100) GaAs.
D.R. Lovell, T. Takebe, T. Yamamoto, M. Inai, K. Kobayashi and
T. Watanabe: To be submitted to JJAP.

Abrupt Heterojunctions of AlGaAs/GaAs Quantum Wells Grown on (111)A GaAs Substrates by Molecular Beam Epitaxy.
T. Yamamoto, M. Fujii, T. Takebe, D. Lovell and K. Kobayashi:
Proc. 18th Int. Symp. GaAs and Rel. Cmpds. IOP (1992).

Presentations.

Ti/Au and Ti Schottky Contacts on Si-doped p-type MBE GaAs on (111)A Substrates.
D.R. Lovell, T. Yamamoto, M. Inai, T. Takebe and K. Kobayashi: Presented at the 39th Spring Meeting of the Japan Society of Applied Physics, Mar. 30/92, Narashino, Japan. Extended Abstract no. 30a-Q-9

GaAs Homojunction Light Emitting Diodes on GaAs (111)A Substrates.
K. Fujita, M. Inai, T. Yamamoto, D. Lovell, T. Takebe and K. Kobayashi: Presented at the 39th Spring Meeting of the Japan Society of Applied Physics, Mar. 30/92, Narashino, Japan. Extended Abstract no. 30p-Za-8

Electrical Characteristics of Lateral p-n Junctions on Patterned (111)A GaAs Substrates.
M. Inai, T. Yamamoto, M. Fujii, D. Lovell, T. Takebe, N. Saitoh and I. Fujimoto: Presented at the 39th Spring Meeting of the Japan Society of Applied Physics Mar. 30/92, Narashino, Japan. Extended Abstract no. 30p-Za-7

Fabrication of a Current Blocking Structure on Patterned (111)A GaAs Substrates by the MBE Growth of GaAs(Si).
M. Inai, T. Yamamoto, M. Fujii, D. Lovell, T. Takebe, K. Kobayashi, S. Hiyamizu and I. Fujimoto: Presented at the 52nd Fall Meeting of the Japan Society of Applied Physics Oct. 9/91, Okayama, Japan. Extended Abstract no. 9p-W-6

Patents.

A Method for Fabricating Non-Rectifying Electrical Contacts on the Surface of Gallium Arsenide.
D. Lovell, T. Takebe, T. Watanabe

INTRODUCTION

This report is a summary of my work with ohmic contacts, Schottky contacts and field effect transistors on n-type and p-type (111)A GaAs. It contains copies of the manuscripts that I have prepared for journal publication in addition to unpublished data and process recipies. I hope that it will serve as a useful guide to those who will continue to study the properties of metals on (111)A GaAs, after I leave.

D. Lovell

July 27, 1992.

CONTENTS

1) OHMIC CONTACTS

1.1) A General Description of Ohmic Contacts.

Ohmic contacts are non-rectifying contacts where current is linearly proportional to the applied voltage, over a finite range of voltages. They are used to inject current into and remove current from a semiconductor. Planar ohmic contacts, where current flows horizontally through the semiconductor, are required for device applications. They are formed by depositing metals onto semiconductor wafers and then annealing the wafers so that some metal atoms diffuse into the semiconductor and form a doped interfacial layer between the bulk of the metal and the bulk of the semiconductor. This forms a low barrier height metal-semiconductor junction. For doping concentrations above 10^{19} cm^{-3}, current flow in an ohmic contact is a tunneling process [1]. For doping concentrations below 10^{19} cm^{-3}, current flows via a mixture of tunneling and thermionic emission [1]. The ohmic contact resistance R_c depends strongly on the carrier concentration of the semiconductor, according to [1]:

$$R_c = \exp\left(\frac{2\sqrt{\epsilon_s m^*}}{h}\right)\left(\frac{\phi_B}{\sqrt{N}}\right) \qquad \Omega \tag{1}$$

where ϵ_s is the dielectric constant of the semiconductor, m^* is the mass of the current carrying species, ϕ_B is the barrier height of the ohmic metal-semiconductor junction and N is the carrier concentration. Ohmic contacts on highly doped semiconductors are preferred for device applications since their R_c is low.

Ohmic contact resistance is measured using a transmission line (TLM) test pattern. The TLM analysis technique is discussed in great detail elsewhere [2,3], and will only be reviewed briefly here. TLM test structures consist of a series of equal area contacts separated by spaces of different lengths. The entire structure sits on an isolated portion of the semiconductor surface. The resistance of each gap is measured by pushing a current across the gap and simultaneously measuring the voltage drop. This measurement requires that 2 probes be used for pushing current and that 2 probes be used for measuring voltage. This ensures that the resistance of an individual probe is eliminated from the measured resistance. (Note that the resistance of 2 probe I-V measurements include the resistance of the probes since a

current and a voltage are being applied and measured with the same piece of metal.) The resistance across each gap is related to the length of each gap by [2,3]:

$$R_t = 2R_c + (\frac{R_s}{W})L \qquad \Omega \tag{2}$$

R_t is the measured resistance and it represents the total resistance of both metal contacts and the semiconductor between them. R_c is the resistance of the contact metal, R_s is the sheet resistance of the semiconductor between the metal contacts, W is the width of the contacts and L is the length of each gap. R_c is determined by plotting R_t versus L and extrapolating a least squares fit of the data to zero length. This resistance intercept equals $2R_c$. R_c is normalized by multiplying it by the the contact width and it is reported in units of Ω-mm.

Specific contact resistivity is often used to characterize ohmic contacts. Specific contact resistivity is defined as follows [1]:

$$\rho_c = (\frac{\partial J}{\partial V})^{-1}|_{V=0} \qquad \Omega - cm^2 \tag{3}$$

ρ_c is resistivity, J is current density and V is voltage. Specific resistivity is measured by using a Kelvin resistor test structure [4,5]. This test structure is different from a TLM test structure, although a TLM structure can be used to give an approximate value of ρ_c, using the following equation.

$$\rho_c = R_c A[\cosh^{-1}(\frac{R_c}{R_e}) \cdot \coth(\cosh^{-1}(\frac{R_c}{R_e}))]^{-1} \qquad \Omega - cm^2 \tag{4}$$

A is the area of the ohmic contact, R_c is the contact resistance and R_e is the end resistance of the ohmic contacts. End resistance [6,7] was derived assuming that the depth of the interfacial layer in an ohmic contact is negligible. For many ohmic contact systems this assumption is not valid which limits the use of end resistance measurements. For example, if end resistance is negative then it is physically meaningless and equation 6 can not be used to calculate ρ_c. All of the R_c data presented in this report were obtained by TLM analysis.

1.2) N-type ohmic contacts.

Ni/AuGe/Au contacts have been studied as ohmic contacts for n-type GaAs. This combination of metals has been used extensively as a n-type ohmic contact on GaAs. The purpose of my experiments with n-type ohmic contacts has been first to establish processes which could be used for my work on Schottky contacts on n-type GaAs and

second to lower the minimum contact resistance of Ni/Ge/Au based ohmic contacts by improving the fabrication technology.

Most of my experiments with n-type ohmic contacts were done by evaporating Ni and AuGe simultaneously in a resistance heat evaporation system. Subsequently, Au was evaporated onto the Ni/AuGe to reduce the resistance of the contact metal. Specific results will now be discussed in detail.

Ni-Ge-Au ohmic contacts are used extensively in the fabrication of electronic and opto-electronic devices on n-type GaAs. The properties of Ni-Ge-Au contacts which have been formed on n-type (100) GaAs by depositing the individual metals separately have been widely reported. The properties of ohmic contacts on n-type (111)A GaAs or on surfaces which are misoriented from the (111)A surface have not been studied extensively although MBE growth of Si doped n-type GaAs layers on (111)A GaAs and on (111)A GaAs which is misoriented by 1^o, 3^o and 5^o toward [100] has been demonstrated[8]. The surface morphology of n-type epitaxial layers grown on (111)A GaAs misoriented by 5^o toward [100] is specular and it is possible to fabricate electronic and opto-electronic devices on this material. Therefore, the properties of Ni-Ge-Au contacts on (111)A GaAs misoriented by 5^o to [100] warrant investigation. In addition, the dependence of contact resistance (R_c) on the thickness of the constituent metal layers and their relative physical positions in ohmic contact metal is not well established. Some works show that contacts which contain a thin layer of Ni, which has been depositied on GaAs prior to AuGe and Au, have low R_c with acceptable uniformity[9-12]. Other works show that contacts which contain an initial layer of Ge also have low R_c and are sufficiently uniform[13-15]. Forming Ni/AuGe/Au contacts by depositing Ni and AuGe simultaneously has not been frequently discussed in the literature eventhough this process simplifies ohmic contact fabrication on n-type GaAs since precise control of the metal layer thicknesses is not required.

In this letter we compare the R_c of equivalent Ni/AuGe/Au ohmic contacts on n-type epi-layers grown using MBE on (111)A GaAs which is misoriented by 5^o toward [100] and on (100) GaAs. From here on (111)A GaAs misoriented by 5^o toward [100] will mostly be referred to as (111)A GaAs.

Si doped n-type epitaxial layers were grown on horizontal Bridgman (H.B.) grown Cr doped semi-insulating (S.I.) (100) GaAs and on H.B. grown Cr doped S.I. (111)A GaAs substrates. A 0.5 μm blanket n^+ layer was grown on one of the (100) sub-

strates. van der Pauw measurements showed that the carrier concentration of this epi-layer was 3.09 X 10^{18} cm^{-3} and that the carrier mobility was 2.04 X 10^3 $cm^2/V{\cdot}s$. On other (111)A and (100) substrates the epitaxial growth structure consisted of a 500 $\AA$ n^+ layer ($n \simeq 3$ X 10^{18} cm^{-3}) grown on a 5000 $\AA$ n^- layer ($n \simeq 2$ X 10^{17} cm^{-3}). The epi-layers on these wafers were grown under conditions which are known to produce n-type GaAs. The n^+/n^- structures are used in the development of recessed gate FETs on (111)A GaAs.

The first step in forming the Ni/AuGe/Au contacts was mesa etching the GaAs. Metals were deposited onto the mesas via lift off lithography. Before metal deposition, the patterned samples were cleaned in a dilute solution of acid. The concentration was fixed at 20 H_2O : 1 acid and HCl, H_2SO_4 and H_3PO_4 were used in each of three comparison experiments where one sample of the n^+/n^- structure on (111)A GaAs and one sample of the n^+/n^- structure on (100) GaAs were processed together in order to accurately compare the ohmic contact resistances on each material. The samples were dipped in the acid solutions for 5 seconds and then rinsed in flowing D.I. H_2O for 3 minutes before being dried with N_2 and loaded into the evaporation system. 0.44 grams of a AuGe eutectic alloy (12% Ge by weight) and 0.07 grams of Ni were evaporated simultaneously from the same boat in a cryogenic pumped resistance heat evaporation system. Evaporation continued until all of the Ni and AuGe was deposited onto the samples, thus preserving the AuGe eutectic composition. The deposition power and the delay time between when the Ni/AuGe liquified and when the deposition began were different in each experiment so that a variety of contact compositions could be studied. Since the thickness of each Ni/AuGe layer was 650 $\AA$ or less, a thicker layer of Au was evaporated onto the samples immediately following the Ni/AuGe deposition in order to lower the resistivity of the contact metal. The samples were at ambient temperature and were rotated while the metals were being deposited. After metal lift off, the samples were alloyed in a quartz furnace with a N_2 ambient at 450C for 5 minutes. Metal layer thicknesses were measured during deposition using a crystal monitor.

Ni/AuGe/Au contacts were also formed on (100) GaAs which had a blanket MBE n^+ layer. This sample was prepared using the same process sequence used in the comparison experiments but it was processed separately. It served as a control from which the R_c of the contacts containing simultaneously deposited Ni/AuGe on n^+ (100) GaAs could be compared to reported R_c data for Ni-Ge-Au contacts formed by

depositing separate metal layers on n^+ (100) GaAs. In addition, another sample of (100) GaAs with a blanket n^+ layer ($n \simeq 3$ X 10^{18} cm^{-3}) was processed separately with the sequence used for the comparison experiments but it was removed from the evaporator following the deposition of a thin layer of Ni/AuGe. After metal lift off current-voltage (I-V) measurements were made to check whether unalloyed, simultaneously depositied Ni/AuGe is ohmic.

Contact resistance data were obtained by using the transmission line (TLM) technique [16,17]. Four probe I-V measurements were made with a Hewlett Packard 4145B Semiconductor Parameter Analyzer. The spaces between the contacts of the TLM structure are nominally 10, 20, 30, 40, 50, 60 and 70 μm, the contact width is 100 μm and the contact length is 70 μm. The contact dimensions and the spaces between contacts on each TLM structure were measured individually with a scanning electron microscope. Resistance versus length data were analysed using least squares regression. The degree of fit of each resistance versus length line to a linear model was between 0.990 and 1.000. The R_c data from the comparison experiments are plotted in Fig. 1 and all the R_c data are listed along with the contact compositions in table I.

The average R_c data within each comparison experiment are very close which shows that R_c does not depend on GaAs crystal orientation and also indicates that ohmic contacts suitable for device applications can be fabricated on n-type (111)A GaAs which is misoriented by 5° towards [100]. The R_c data of the third comparison experiment are higher than those of the first two comparison experiments and this appears to be caused by differences in the surface cleaning processes. Ni/AuGe/Au ohmic contacts on H_3PO_4 treated n-type GaAs have higher contact resistances than similar contacts on n-type GaAs which has been cleaned with dilute solutions of H_2SO_4 and HCl. This suggests that phosphorous based compounds are attached to the semiconductor surface after rinsing GaAs following surface cleaning with H_3PO_4. During the metal deposition and alloying processes these compounds are incorporated into the contact metal.

Table I

R_c of Ni/AuGe/Au ohmic contacts on *n*-type (111)A and (100) epi-layers.

Experiment Number	$R_{c(111)A}$ Ω-mm	$R_{c(100)}$ Ω-mm	Contact Composition	Surface Cleanser
1)	0.035 ± 0.009	0.030 ± 0.010	650 Å Ni/AuGe + 2534 Å Au	HCl
2)	0.037 ± 0.009	0.038 ± 0.004	255 Å Ni/AuGe + 1558 Å Au	H_2SO_4
3)	0.056 ± 0.008	0.055 ± 0.004	585 Å Ni/AuGe + 2119 Å Au	H_3PO_4
(100) Control sample		0.020 ± 0.004	282 Å Ni/AuGe + 1979 Å Au	HCl
(100) Control sample (After 48 hours at 400°C.)		0.030 ± 0.004	282 Å Ni/AuGe + 1979 Å Au	HCl

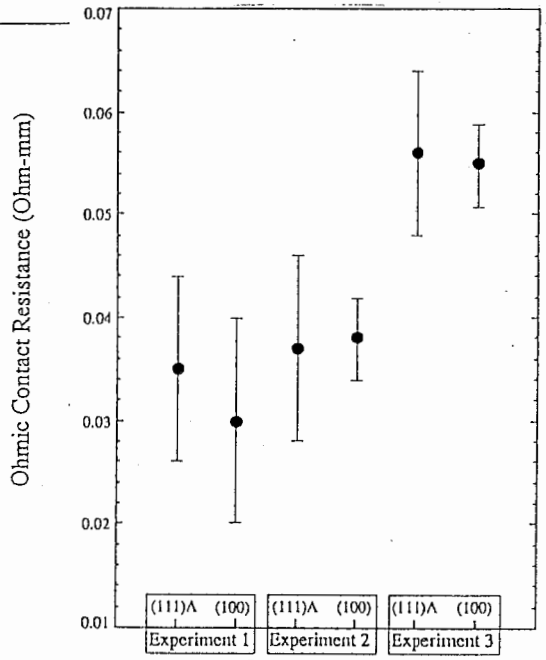

Fig. 1 - Ohmic contact resistances from the comparison experiments. All I-V measurements were made at 295.5 K.

Higher R_c variations are observed for contacts on (111)A GaAs in the last two comparison experiments. The increase in R_c variation between the (100) and (111)A orientations is 0.004 to 0.005 Ω-mm. Non-uniformities in the physical distribution of the contact metal across the (111)A surfaces account for the higher R_c variations. This reflects differences in the smoothness of the (111)A and (100) GaAs surfaces after being cleaned with dilute H_2SO_4 and H_3PO_4. The R_c variations in the first comparison experiment are virtually identical implying that the smoothness of these surfaces is equally affected by dilute HCl.

The R_c of Ni/AuGe/Au contacts on the (100) GaAs control sample is 0.020 ± 0.004 Ω-mm. After storage at 400°C for 48 hours this R_c was remeasured and found to be 0.030 ± 0.004 Ω-mm. The difference in R_c which is observed before and after thermal storage is 0.010 Ω-mm indicating that ohmic contacts containing a layer of simultaneously deposited Ni/AuGe are thermally stable. The control sample R_c data is lower than the R_c data from the (100) samples used in the comparison experiments. This is explained by the difference in epitaxial structures on the two (100) GaAs wafers. The control data was obtained from contacts on a 5000 Å n^+ epi-layer which was grown on semi-insulating (100) GaAs. The R_c data from the comparison experiments were obtained from contacts on a 500 Å n^+ layer situated on a higher resistivity 5000 Å n^- layer. The portion of the measurement current which passed through the buried n^- layer encountered this higher resistance which increased the voltage drop between contacts on the TLM structures. The control sample R_c is typical for contacts which contain a layer of simultaneously deposited Ni/AuGe.

R_c values of 0.11 Ω-mm[11] and 0.074 Ω-mm[14] have been reported for Ni(50 Å)/AuGe(1000 Å)/Ni(300 Å)/Au(500-1000 Å) contacts, on a (100) GaAs substrate doped by SiF^+ implantation, and Ge(50 Å)/Ni(50 Å)/AuGe(500 Å)/Ag(300 Å)/Au(1100 Å) contacts, on a single layer of n^+ Si doped MOCVD grown GaAs. The associated carrier concentrations are 1.5 X 10^{18} cm^{-3} and 6 X 10^{18} cm^{-3} respectively. Since the R_c of contacts which contain a simultaneously depositied Ni/AuGe layer are lower than these values it is believed that control of the position and thickness of Ni and Ge are not necessary in forming low R_c ohmic contacts on MBE grown *n*-type GaAs. Furthermore, contacts fabricated with simultaneously deposited Ni/AuGe are tolerant to variations in metal layer thickness and surface

treatments. The R_c data in table I vary from $\pm$ 8 % to $\pm$ 33 % of the average R_c values for each experiment. This is comparable to reported R_c variations for contacts which contain Ni, Ge and Au [9–11,13,14].

Ni_2AsGe is responsible for the non-rectifying electrical behaviour of Ni/AuGe/Au contacts [9–13] and Ni_2AsGe forms when the contact metallization is alloyed[9,10,12]. During the alloy process a NiAs phase forms near the surface of the GaAs substrate and a NiGe phase forms in the upper regions of the contact metal, away from the GaAs surface and Ni_2AsGe is formed when Ge diffuses out of NiGe and into NiAs[12]. The extent to which Ni, As and Ge metals react with the GaAs is limited when the metals are deposited individually because the substrate and one of the metal layers will always be separated by another metal. By simultaneously depositing Ni and AuGe onto GaAs, Ni, As and Ge are free to react physically and chemically right from the beginning of contact fabrication. Fig. 2 shows that simultaneously deposited Ni/AuGe is not ohmic. However, it presumably contains NiAs and NiGe, among other metal phases, which are in direct contact with the GaAs surface. The low contact resistances which result from this process suggest that Ni_2AsGe is formed when contacts containing a co-deposited Ni/AuGe layer are alloyed. The simultaneous Ni/AuGe deposition technique ensures that the Ni-As-Ge compounds formed during metal evaporation distribute across the GaAs surface, which is necessary in achieving uniform R_c. Since the alloyed metal phases penetrate into the GaAs bulk, conduction is not controlled by properties of the GaAs surface. This explains why the R_c values of Ni/AuGe/Au ohmic contacts fabricated on both (111)A and (100) GaAs are not affected by differences in surface chemistry.

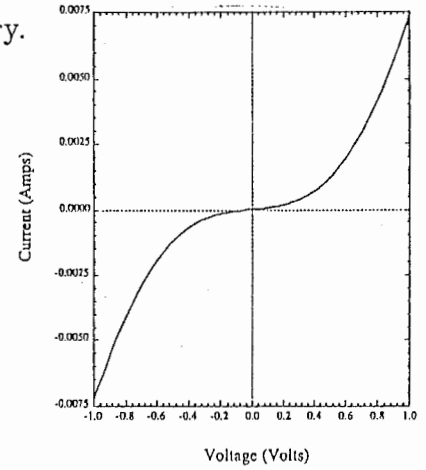

Fig.2 - Current versus voltage for a 388 $\AA$ layer of unalloyed, simultaneously deposited Ni/AuGe. Measurements were made at 295.5 K between two 225 μm X 270 μm metal pads separated by a 5 μm space.

In conclusion, we compared the contact resistance of equivalent Ni/AuGe ohmic contacts on (111)A GaAs misoriented by 5° toward [100] and on (100) GaAs and have found no appreciable difference. While the contact resistance of alloyed contacts on MBE grown *n*-type GaAs is not affected by differences in the semiconductor surface chemistry, R_c uniformity may be affected by differences in GaAs surface chemistry depending on the surface cleaning process. In addition, low resistance, thermally stable Ni/AuGe/Au ohmic contacts have been fabricated on *n*-type GaAs, after HCl surface cleaning, by depositing Ni and a AuGe eutectic alloy simultaneously from the same boat of a resistance heat evaporation system, subsequently depositing Au and then alloying the metal at 450°C. Formation of a variety of metal phases during metal deposition, particularly NiAs and NiGe from which Ni_2AsGe may be easily formed, is believed to explain why ohmic contacts that contain a layer of simultaneously evaporated Ni and AuGe have low R_c.

1.3) P-type ohmic contacts.

The purpose of my experiments with ohmic contacts on p-type GaAs was to develop processes which could be used to fabricate the Schottky diodes necessary for my research of the electrical properties of Schottky barriers on (111) GaAs. All of my work focussed on using Mn/Au contact metallization.

An extensive study of Mn/Au ohmic contacts has been reported by Dubon-Chavallier [18] *et. al.*. Compared to Zn/Au contacts, Mn/Au contacts exhibit lower contact resistivity [18,19]. Also, Mn does not appear to diffuse into GaAs as much as Zn does [18,19]. Diffusion of the dopant species needs to be minimized in devices like heterojunction bipolar transistors where the p-type ohmic layers are thin, like 1000 Å. If contact metal dopants diffuse through such layers device performance will be degraded.

The issue of device performance does not concern ATR at this moment since we are not developing specific devices. However, I did not want to develop processes which could not be used successfully in device development work. So I chose to work with Mn based p-type ohmic contacts because I believe that they offer advantages to the traditional Zn/Au metallization.

The first matrix experiment was done to determine the best alloy time and temperature for Au/Mn contacts consisting of 4 weight % Mn. A 0.5 μm Be doped GaAs layer was grown on (100) GaAs by MBE. van der Pauw measurements showed that the conductivity was p-type, the carrier concentration was 1.32×10^{19} cm^{-3} and the carrier mobility was 72.2 $cm^2/Vsec$. Ohmic TLM test structures were first formed by mesa etching. Mn and Au were deposited using lift off lithography. No surface cleaning was done before loading the samples into the deposition system. The target metal thickness were 208 $\AA$ for Mn and $\AA$ for Au and the target Mn content was 3.85 % by weight. The actual Mn thickness was 221 $\AA$ and the Au thickness was 2154 $\AA$. The Mn content was 3.80 % by weight. One sample was left unalloyed and the remaining 5 samples were alloyed at 400°C for differing lengths of time, varying from 5 to 17 minutes. R_c data were obtained using the TLM method and they and are shown in table II.

Table II

Effect of Alloy time on R_c for Au/Mn contacts.

Alloy Conditions	R_c (Ω-mm)
Unalloyed	0.117
400°C/5 min	0.099
400°C/7 min	0.087
400°C/9 min	0.092
400°C/11.6 min	0.094
400°C/17 min	0.101

Two additional samples were prepared and they were alloyed for 7 minutes at different temperatures. R_c data is contained in table III.

Table III

Effect of Alloy Temperature on R_c for Au/Mn contacts.

Alloy Conditions	R_c (Ω-mm)
375°C/7 min	0.099
400°C/7 min	0.087*
425°C/7 min	0.099

* comes from the previous table.

The lowest R_c value in table III resulted when the contacts were alloyed at 400°C for 7 minutes. These alloy conditions give the lowest R_c values of all the alloy conditions studied in tables II and III. The R_c values are all in the vicinity of 0.1 Ω-mm which indicates that small variations in the alloying conditions do not drastically increase R_c on highly doped p-GaAs. One important feature of Mn/Au contacts is that they do not need to be alloyed in order to become non-rectifying. Low resistance ohmic contacts can be formed simply by depositing the Mn and Au in the right proportions.

Additional experiments were done to compare Mn/Au ohmic contact properties on p-type epitaxial (111)A GaAs and on p-type epitaxial (100) GaAs. One goal of this work was to study the effect of reducing the alloy time and increasing the alloy temperature. As a control, one sample of highly doped (100) material was included in this experiment. Sample preparation was the same as described in the appendix. These samples were cleaned in 10:1 H_2O:HCl for 5 seconds and then rinsed in flowing D.I. H_2O for 3 minutes before ohmic metal deposition. The results are shown in table IV.

Table IV
Mn/Au Ohmic contact comparison experiment

Sample/ Carrier Concentration (cm^{-3})	Contact Composition	Alloy Conditions	R_c Ω-mm
(100) $1x10^{19}$	172Å Mn/1586Å Au	450°C/2 min	0.094
(111)A $3x10^{17}$	172Å Mn/1586Å Au	450°C/3 min	0.824
(100) $3x10^{17}$	172Å Mn/1586Å Au	450°C/3 min	0.644
(111)A $3x10^{17}$	220Å Mn/2010Å Au	450°C/4 min	1.91
(100) $3x10^{17}$	220Å Mn/2010Å Au	450°C/4 min	2.48

I have found that Mn/Au ohmic contacts on low doped p-GaAs are very sensitive to alloy time, as is indicated in table IV.

2) SCHOTTKY CONTACTS

2.1) A Brief Description of Schottky Contacts.

Schottky contacts are rectifying contacts where only very low currents can flow over a finite range of voltages. They consist of metals on specular semiconductor surfaces, where the carrier concentration of the semiconductor is $5x10^{17}$ cm^{-3} or less. In order to establish thermal equillibrium, the Fermi level of both materials must be equal. This results in charge exchange between the metal and the semiconductor which causes a built-in voltage to be present near the interface. This voltage is distributed between the semiconductor surface and a finite distance into the semiconductor, typically a few hundred angstroms. Free carriers do not exist in this space and it is therefore known as a depletion region. Schottky contacts are effectively barriers to current flow. A representative linear I-V characteristic for a Ni/Au Schottky contact on n-type (111)A GaAs is shown in Fig. 3.

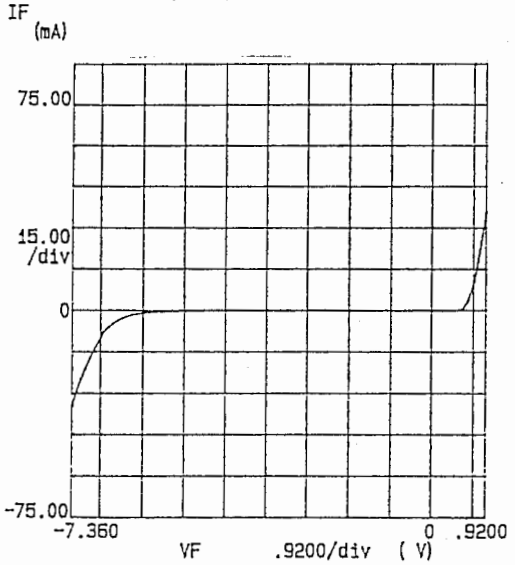

Fig. 3 - Linear I-V characteristic for Ni/Au on n-type (111)A GaAs.

The current density Schottky contacts is described by:

$$J = A^*T^2 \exp(\frac{-q\phi_b}{kT} \exp(\frac{qV}{nkT}), \quad where V > (\frac{kT}{q}) \tag{5}$$

J is the current density in the contact, T is temperature, q is the electron charge, ϕ_b

is the barrier height of the contact, k is the Boltzmann constant, V is applied voltage and n is the ideality factor. The physics of current transport at metal semiconductor junctions is described in great detail in Ref. 23 and general aspects of this subject are not presented in this report.

2.2) Schottky Contacts on P-type (111)A GaAs.

The properties of metal-GaAs interfaces have been studied in great detail, because research on the dependence of Schottky barrier heights upon metal work functions is crucial in increasing the applicability of GaAs electronic devices, particularly GaAs Field Effect Transistors (FET). Since most studies of Schottky barriers on GaAs have been conducted on (100) GaAs substrates or on epitaxial layers grown on (100) GaAs substrates, the properties of metal contacts on other GaAs surfaces, such as the (111)A surface, have not been widely reported. We have recently succeeded in growing p-type Si-doped GaAs layers with mirror-like surfaces and reproducible electrical properties on (111)A GaAs substrates, using molecular beam epitaxy (MBE)[20]. We have begun to investigate the properties of opto-electronic devices constructed on MBE grown lateral p-n-p junctions on (111)A GaAs[21]. It is now important to study the properties of electrical contacts on epitaxial GaAs, with carrier concentrations suitable for FET fabrication, grown on (111)A GaAs using MBE.

In this letter, we investigate the properties of Ti/Au Schottky contacts deposited on a p-type Si-doped MBE GaAs layer grown on a (111)A GaAs substrate and compare them to equivalent contacts on a p-type Be-doped MBE GaAs layer grown on a (100) GaAs substrate.

The diodes used in this study were fabricated on p-type epitaxial GaAs which was grown on Cr-doped, horizontal Bridgman grown, semi-insulating (111)A and (100) GaAs substrates. The first step in diode preparation was the isolation of portions of the epi-layers using mesa etching. Subsequently, Mn/Au ohmic contacts consisting of 4 weight % Mn were evaporated onto a photoresist lift off pattern. After metal lift off, the samples were alloyed at 450°C for 3 minutes in a N_2 ambient. The Schottky barriers were formed, via lift off, by evaporating 100 $\AA$ of Ti, followed directly by 2000 $\AA$ of Au. The deposition rate of Ti was 1 $\AA$ per second and the Au deposition rate was 10 $\AA$ per second. The Schottky junctions consisted of Ti on p-GaAs. Au was deposited in order to prevent oxidation of the Ti and to lower

the series resistance of the Schottky diodes. Immediately before loading the samples into the evaporator for Schottky metal deposition, one sample of each material was cleaned in 20:1 H_2O:H_2SO_4 for 10 seconds at room temperature and one sample of each material was cleaned in 20:1 H_2O:H_3PO_4 for 10 seconds at room temperature. All samples were then rinsed in flowing D.I. H_20 for 3 minutes and dried with N_2. All samples were processed simultaneously in order to eliminate process variability from the experimental results. The Schottky and ohmic contacts were deposited using resistance heat evaporation. The substrates were at ambient temperature during all metal deposition runs.

Carrier concentrations and carrier mobilities were measured using the van der Pauw technique, which also confirmed p-type conductivity in both epi-layers. Current-voltage (I-V) measurements were made with a Hewlett Packard 4145B Semiconductor Parameter Analyzer and capacitance-voltage (C-V) measurements were made with a Hewlett Packard 4280A Capacitance Meter. C-V measurements were made at 1 MHz with an ac signal of 30 mV.

Barrier heights were calculated from forward bias I-V data using the thermionic emission model for current transport at a metal-semiconductor interface[22].

$$\phi_{Bp} = \frac{kT}{q} \ln \frac{A^{**}T^2}{|J_s|}, \qquad for \;\; V > 3\frac{kT}{q} \tag{6}$$

A^* is the effective Richardson constant and J_s is the forward current density at zero bias. J_s values were determined by a least squares fit of the linear portion of the I-V data above $V = 3\frac{kT}{q}$. The effective Richardson constants for p-type (111)A GaAs and p-type (100) GaAs are different due to the differences in the light hole effective mass (m^*_{lh}) and the heavy hole effective mass (m^*_{hh}) between these two surfaces. For p-type semiconductors, A^{**} is calculated by using[22,23]:

$$\frac{A^{**}}{A} = \frac{m^*_{lh} + m^*_{hh}}{m_o}, \qquad where \;\; A^{**} = \frac{4\pi m^* q k^2}{h^3} \tag{7}$$

A is the value of A^{**} calculated with m^* equal to m_o, k is the Boltzmann constant, h is the Planck constant and m_o is the electron rest mass, $m^*_{hh(111)A} = 0.90m_o$ [5] and $m^*_{lh(111)A} = 0.08m_o$ [6]. For p-type (111)A GaAs $A^{**} = 117.8$ $Acm^{-2}K^{-2}$. For p-type (100) GaAs $A^{**} = 74.4$ $Acm^{-2}K^{-2}$ [22,26].

A log-linear plot of current density versus forward bias for the diodes used in this study is shown in Fig 4. Lines are fitted to the data which lie above $V = 3\frac{kT}{q}$. The current densities of Ti/Au contacts on the epi-layer grown on (111)A GaAs are

consistently lower than for identical contacts on the epi-layer grown on (100) GaAs. This results in lower J_s values and higher barrier heights for contacts on the (111)A epi-layer. Although the current densities of contacts on H_3PO_4 treated surfaces are slightly lower than on H_2SO_4 treated surfaces, the I-V barrier heights are not greatly affected by the different surface cleaning processes.

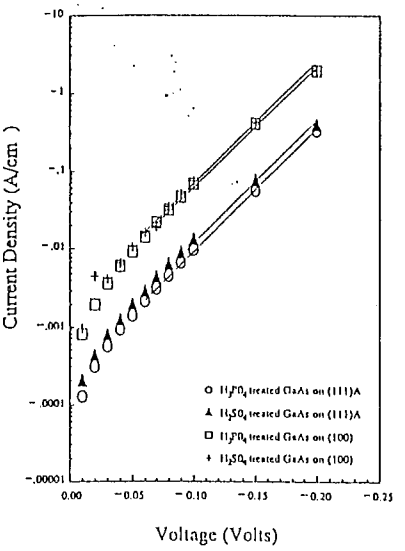

Fig. 4. Logarithm of forward current density versus forward bias for Ti/Au Schottky contacts on p-type epitaxial GaAs grown on (111)A and (100) GaAs, measured at 295.5 K.

Assuming one-sided step-junction behaviour of the metal-GaAs junctions, the barrier heights were also calculated from reverse bias C-V data using[22]:

$$\phi_{Bp} = |V_i| + V_p \tag{8}$$

V_i (or diffusion potential) is the voltage intercept from a least squares fit of $1/C^2$ versus reverse bias data. V_p is the difference between the Fermi level and the valence band in the bulk of the semiconductor. Based on the sample carrier concentrations and the m^*_{lh} and m^*_{hh} data for GaAs[22,24,25], V_p values for p-type epi-layers on (111)A and (100) GaAs are calculated using[22]:

$$V_P = E_f - E_v = \frac{kT}{q} \ln \frac{Nv}{Na} \tag{9}$$

Nv is the density of states in the valence band and Na is the acceptor concentration of the GaAs. For the epi-layer on (111)A GaAs $V_p = 0.110$ eV and for the epi-layer on (100) GaAs $V_p = 0.075$ eV.

A plot of $1/C^2$ versus reverse bias for the diodes used in this study is shown in Fig 5. Higher diffusion potentials are observed for Ti/Au contacts on epitaxial

GaAs grown on (111)A GaAs and this results in higher barrier heights for Ti/Au contacts on GaAs grown on (111)A GaAs. The diffusion potentials of contacts on H_2SO_4 treated GaAs are higher than those observed on H_3PO_4 treated GaAs. The difference in surface cleaning processes has a small, measureable effect on the C-V barrier heights.

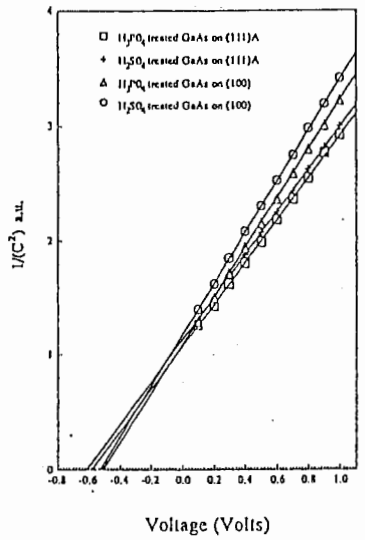

Fig. 5. 1/(Capacitance)^2 versus reverse bias for Ti/Au Schottky contacts on p-type epitaxial GaAs grown on (111)A and (100) GaAs, measured at 295.5 K.

Table V Epitaxial layer characteristics and corresponding electrical properties of the Ti/Au Schottky contacts.

	On (111)A GaAs		On (100)GaAs	
Characteristics of the p-type epitaxial layers.				
Carrier Concentration (cm^{-3})	2.85×10^{17} (Si)		3.65×10^{17} (Be)	
Carrier Mobility ($cm^2/V\cdot s$)	179		157	
Layer Thickness (μm)	0.5		1.6	
Electrical data from Ti/Au contacts on p-type epitaxial GaAs grown by MBE.				
Surface cleaning reagent	H_2SO_4	H_3PO_4	H_2SO_4	H_3PO_4
J_s (A/cm^2)	-4.52×10^{-4}	-2.69×10^{-4}	-2.23×10^{-3}	-1.96×10^{-3}
Ideality factor n	1.09	1.06	1.06	1.05
$\phi_{B_p}^{I\text{-}V}$ (eV)	0.61	0.62	0.56	0.56
V_i (V)	−0.61	−0.58	−0.53	−0.51
$\phi_{B_p}^{C\text{-}V}$ (eV)	0.72	0.69	0.61	0.59
$\Delta\phi_{B_p}(\phi_{B_p}^{C\text{-}V}-\phi_{B_p}^{I\text{-}V})$ (eV)	0.11	0.07	0.05	0.03

Notes:
1) $(kT/q)=0.0255$ eV at 295.5 K.
2) All measurements were made on 7.01×10^{-5} cm^2 diodes.
3) The uncertainty in ϕ_{B_p} values is 0.01 eV, except for $\phi_{B_p}^{I\text{-}V}$ on H_2SO_4 treated GaAs on (111)A GaAs. This uncertainty is 0.02 eV.
4) The uncertainty in the n values is 0.005.

Epi-layer characteristics and a summary of the results shown in Figs. 4 and 5 are contained in Table V. The main result is that the Schottky barrier heights of Ti/Au contacts on p-type epitaxial GaAs grown on (111)A GaAs are consistently higher than the barrier heights of identical contacts on p-type epitaxial GaAs grown on (100) GaAs. The C-V barrier heights are 0.11 eV - 0.10 eV higher. The I-V barrier heights are 0.06 eV - 0.05 eV higher.

The effect of the difference in carrier concentration between the samples is explained as follows. The carrier concentration of the Si-doped epi-layer on (111)A GaAs is about 1.3 times lower than the Be-doped epi-layer on (100) GaAs. A I-V barrier height of 0.56 eV for Ti on p-type (100) GaAs with a carrier concentration of $8x10^{16}$ cm^{-3} has been reported by Waldrop[26]. The carrier concentration of the (100) epi-layer used in our experiment is more than four times higher than that used by Waldrop and yet the I-V barrier heights on our (100) epi-layer agree exactly with his value. Therefore the smaller difference between the carrier concentrations of the (111)A epi-layer and the (100) epi-layer has no influence on the difference in the Ti/Au barrier heights. Differences in the properties of the Ti/Au contacts may be solely attributed to differences in the surface crystal structure between the (111)A epi-layer and the (100) epi-layer. Agreement between our I-V barrier height data for Ti/Au on a p-type epi-layer on (100) GaAs and the I-V barrier height for Ti on p-type (100) GaAs, reported by Waldrop, also shows that Ti governs the electrical properties of the metal-semiconductor barrier in the Ti/Au contacts.

A comparison between our data and the ideal dependence of Schottky barrier heights on metal work functions for p-type GaAs, using data reported by Duke and Mailhiot[27], is shown in Fig. 6. The solid line represents the dependence of Schottky barrier heights on metal work functions for metal - p-GaAs interfaces where the defect densities are low enough to have no influence on the barrier heights. The vertical dotted line connects the relation between Schottky barrier heights to the metal work function of Ti, indicating that the highest possible barrier height for Ti on p-GaAs is about 1.11 eV. The horizontal dotted lines show the range between the highest ${\phi_{Bp}}^{C-V}$ and the lowest ${\phi_{Bp}}^{I-V}$ which are observed for Ti/Au contacts on each epi-layer. For Ti/Au on the (111)A epi-layer 0.72 eV $\geq \phi_{Bp} \geq$ 0.61 eV. For Ti/Au on the (100) epi-layer 0.61 eV $\geq \phi_{Bp} \geq$ 0.56 eV.

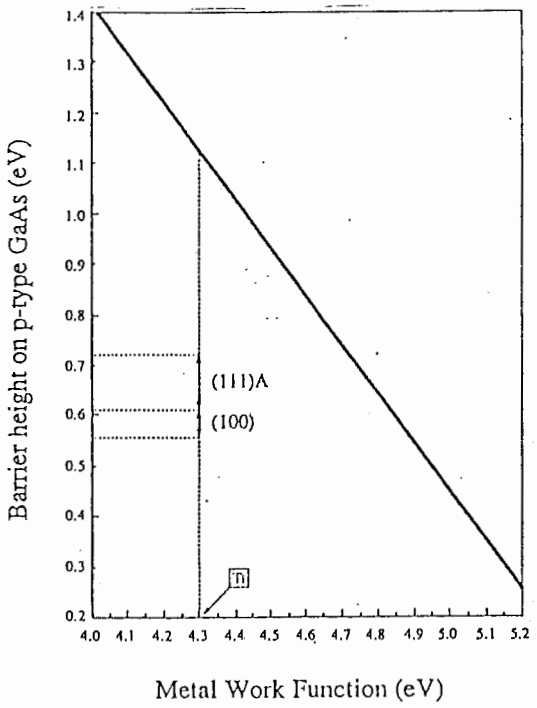

Fig. 6. The ideal relation between Schottky barrier height and metal work function for p-type GaAs. The horizontal dotted lines indicate the range between the highest and the lowest barrier height observed on each epitaxial layer. The vertical dotted line connects the ideal Schottky relation to the work function of Ti, which is 4.3 eV [22].

A lower defect density at the Ti-GaAs interface of the Ti/Au contacts on the epi-layer on (111)A GaAs qualitatively explains why the barrier heights of Ti/Au contacts on this material are closer to the ideal Schottky relation and consistently higher than the barrier heights of identical contacts on the epi-layer grown on (100) GaAs. The term defect density refers to three phenomena. The first phenomenon is surface states which exist at the GaAs surface prior to metal deposition. The second is disruptions in the surface crystal structure of GaAs due to radiation damage encountered during the metal deposition process. The third is the products of chemical reactions that occur at metal-GaAs interfaces during metal deposition. Since the Schottky contacts used in this work were all deposited together, it is believed that the physical disruption of both GaAs surfaces during metal deposition was identical. Differences in the electrical properties of the Ti/Au contacts are due to both differences in the surface state densities of the p-type epi-layers on (111)A and (100) GaAs and differences in the chemical reactions which occur at the Ti-GaAs interfaces of Ti/Au contacts on these epi-layers. The surface state density and surface

reactivity of GaAs surfaces depend on surface crystal structure.

The surface of MBE grown (111)A GaAs is predominantly terminated with Ga atoms. The surface of MBE grown (100) GaAs is terminated with both Ga and As atoms. As surface atoms have an unshared pair of electrons which are free to react with metal overlayers. Since Ga surface atoms have no free electrons, Ga can not react easily with metal overlayers. The Schottky barrier heights of contacts on Ga terminated GaAs are closer to the ideal Schottky relation, compared to the barrier heights of equivalent contacts on a surface containing As, because surface Ga atoms do not react extensively with metal overlayers. This leads to metal-GaAs interfaces which are freer of chemical compounds that could distort the thermionic emission process. The higher reactivity of As terminated GaAs has been discussed previously by Chang *et al.*[28]. Xu *et al.*[29] have shown that Ti reacts with As on (100) GaAs to form TiAs.

The ideality factors in table V are calculated based on data in Fig. 4 using:[22]

$$n = \frac{q}{kT}\frac{\Delta V}{\Delta \ln J_s} \tag{10}$$

Rideout and Crowell have established the following relation between the ideality factor and image force barrier lowering, or $\Delta\phi_B$, when thermionic emission dominates conduction in a metal-semiconductor contact[30], as is the case for Schottky contacts.

$$\frac{1}{n}|_{thermionic} = 1 - \frac{\Delta\phi_B}{4E_b}, \qquad where \quad E_b = \frac{N_a q^2 W^2}{2k_s\epsilon_o} \tag{11}$$

N_a is the semiconductor carrier concentration, W is the depth of the depletion region beneath the metal contact, k_s is the dielectric constant of the semiconductor and ϵ_o is the vacuum permittivity. The C-V barrier height of equation 10 represents the theoretical barrier height of a metal-semiconductor contact. The I-V barrier height represents the minimum energy for thermionic emission and it does not necessarily equal the C-V barrier height. It may be lower. Therefore the difference in C-V and I-V barrier heights (ie. $\Delta\phi_{Bp}$) is a measure of barrier lowering.

On each epi-layer, where E_b of equation 11 is a constant, the larger barrier lowering observed for H_2SO_4 treated GaAs resulted in higher ideality factors, as predicted by equation 11.

On each epi-layer, the diffusion potentials of contacts on H_2SO_4 treated GaAs are higher than for H_3PO_4 treated GaAs. This means that the interface charge density of Ti-GaAs junctions on samples treated with H_2SO_4 is higher. Excess charge in the

junctions explains why the current density of contacts on H_2SO_4 treated GaAs is also slightly higher compared to contacts on H_3PO_4 treated GaAs. Since this extra charge causes both higher diffusion potentials and higher current densities it therefore causes larger differences between C-V and I-V barrier heights. This explains why larger barrier lowering is observed for contacts on H_2SO_4 treated GaAs, which in turn explains why contacts on H_2SO_4 treated GaAs have higher ideality factors. Different surface treatments may cause differences in the surface stoichiometry of GaAs. Phosphorous and sulphur based impurities may have been left on the GaAs surfaces prior to metal deposition. The increase in charge density in contacts on H_2SO_4 treated GaAs may be influenced by both of these phenomenon although this can not be quantified. We show that surface cleaning with dilute H_3PO_4 produces contacts with lower ideality factors, which therefore represent more ideal metal-semiconductor junctions.

In conclusion, we compared the Schottky barrier heights of Ti/Au contacts on p-type epitaxial GaAs layers grown on (111)A and (100) GaAs substrates and have shown that contacts on epitaxial GaAs on (111)A GaAs have higher barrier heights. Differences in the barrier heights of the Ti/Au contacts on different GaAs surfaces may be qualitatively explained by the fact that Ga terminated GaAs surfaces are less reactive with metals, compared to surfaces which contain As. This results in lower defect densities at metal - Ga terminated GaAs interfaces. We have also studied the effect of cleaning GaAs surfaces with dilute solutions of H_3PO_4 and H_2SO_4. Surface cleaning with dilute H_3PO_4 results in more ideal metal-semiconductor interfaces.

The Ti/Au contacts discussed above were fabricated on the surface of MBE p-type (111)A GaAs. Table VI contains data for Pt, Ni and Cr contacts which were formed epitaxial p-type GaAs which was recessed. The results in table VI will be discussed at the end of the next section.

Table VI Properties of Schottky Contacts on p-type (111)A GaAs.

Metal	$\phi_{Bp}{}^{I-V}$ eV	J_s A/cm^2	n	V_{bi} V	$\phi_{Bp}{}^{C-V}$ eV	$\Delta\phi_{Bp}$ eV
Pt	0.29	7.28 X 10^0	≥ 2	—	—	—
Ni	0.49	5.04 X 10^{-3}	≥ 2	0.49	0.57	0.08
Cr	0.44	2.15 X 10^{-2}	≥ 2	0.62	0.70	0.26

2.3) Schottky Contacts on N-type (111)A GaAs.

The high surface state density which is characteristic of GaAs leads to a relatively weak dependence of Schottky barrier height upon metal work function for metal-GaAs contacts. Most studies describing the properties of rectifying contacts on n-type GaAs present data for the (100) GaAs surface, which is one of the GaAs surfaces that contains arsenic atoms. In contrast, the electrical properties of rectifying contacts on n-type (111)A GaAs, a surface that is gallium terminated, have not been widely reported. Since the gallium atoms on the (111)A surface are in a threefold bonding configuration there are no free electrons which can react with metal overlayers. Arsenic atoms on the (100) surface have unshared electrons that are free to react with metal overlayers. The lower reactivity of the (111)A GaAs surface is believed to result in lower interface surface state densities in metal-(111)A GaAs contacts, compared to contacts on GaAs surfaces which contain arsenic atoms.

Epitaxial growth of Si doped n-type GaAs on (111)A GaAs substrates and on (111)A GaAs substrates which are misoriented by 1^o, 3^o and 5^o toward [100] using molecular beam epitaxy (MBE) has been demonstrated[31] and specular epi-layers with reproducible electrical properties can be grown routinely on (111)A substrates which are misorented by 5^o toward [100]. It is therefore possible to study the properties of rectifying contacts on n-type (111)A GaAs with epitaxial growth structures and diode fabrication processes that are used to develop electronic and opto-electronic devices.

This letter reports the first observations of Schottky barrier heights on n-type Si-doped MBE GaAs grown on (111)A GaAs. By fitting a straight line to the Schottky barrier height versus metal work function data for Pt, Ni and Cr the surface state density of the n-type epitaxial layer has been estimated.

The diodes used in this study were fabricated on n-type epitaxial GaAs which was grown by molecular beam epitaxy on Cr-doped, horizontal Bridgman, semi-insulating (111)A GaAs which is misoriented by 5^o towards [100]. The epitaxial structure consists of a 500 $\AA$ n^+ layer ($n \simeq 3$ X 10^{18} cm^{-3}) grown on a 5000 $\AA$ n^- layer. The carrier concentration of the n^- layer was found to be 2.04 X 10^{17} cm^{-3} using the van der Pauw technique and this also confirmed n-type conductivity.

The first step in diode fabrication was device isolation using mesa etching. Ohmic contacts were formed by depositing the Ni/AuGe/Au onto a photoresist lift off pattern and after metal lift off the samples were alloyed at 450°C for 5 minutes in a N_2 ambient. The Schottky barriers were also formed using metal lift off. In order to deposit the Schottky metals on the buried n^- layer, the samples were etched in 2:8:1000 HF:H_2O_2:H_2O while the lift off photoresist pattern was in place. The n^+ material in the exposed regions of the photoresist pattern was removed thus forming a recess into which the Schottky metals could be deposited. The samples were then cleaned in 20:1 H_2O:H_3PO_4 for 10 seconds at room temperature, rinsed in flowing D.I. H_2O for three minutes, dried using N_2 and immediately loaded into a cryogenically pumped, resistance heat evaporator. Three samples were fabricated separately and the Schottky contacts consisted of Pt(200 $\AA$)/Au(2000 $\AA$), Ni(200 $\AA$)/Au(2000 $\AA$) and Cr(200 $\AA$)/Au(2000 $\AA$). Au was deposited in order to prevent oxidation of the 200 $\AA$ barrier metal layers and to lower the diode series resistance. The samples were at ambient temperature and were rotated during all metal deposition runs.

Capacitance-voltage (C-V) measurements were made from 0 to -1 volts using a Hewlett Packard 4280A Capacitance Meter. The measurement frequency was 1 MHz and the amplitude of the ac signal was 30 mV. Current-voltage (I-V) measurements were made from 0 to 0.5 volts using a Hewlett Packard 4145B Semiconductor Parameter Analyzer. Barrier heights were calculated from C-V data using[32)]

$$\phi_{Bn} = V_{bi} + V_n \tag{12}$$

V_{bi} is the voltage intercept from a least squares fit of $1/C^2$ versus reverse bias data and V_n is the difference between the Fermi level and the conduction band in the bulk

of the semiconductor. Based on the sample carrier concentration V_n equals 0.02 eV. Barrier heights were also calculated by analysing the I-V data with the thermionic emission model for current transport at a metal-semiconductor interface[32].

$$\phi_{Bn} = \frac{kT}{q} \ln \frac{A^{**}T^2}{J_s} \quad for \;\; V > 3\frac{kT}{q} \tag{13}$$

J_s, the forward current density at zero bias, was determined by a least squares fit of the linear portion of the forward bias I-V data above V = 3(kT/q). T represents the measurement temperature and A^{**} is the effective Richardson constant, which equals 8.16 $A \cdot cm^{-2} \cdot K^{-2}$ for *n*-type (111)A GaAs[32]. The results are contained in Table VII.

Table VII

Electrical Properties of Pt, Ni and Cr Schottky Contacts on *n*-type (111)A GaAs.

Metal	$\phi_{Bn}{}^{C-V}$ (eV)	V_{bi} (V)	$\phi_{Bn}{}^{I-V}$ (eV)	J_s (A/cm^2)	n	$\Delta\phi_{Bn}$ (eV)	ϕ_{metal} (eV)
Pt	0.90	0.88	0.73	3.04 X 10^{-7}	1.15	0.17	5.68
Ni	0.87	0.85	0.67	2.63 X 10^{-6}	1.18	0.20	5.27
Cr	0.68	0.66	0.56	2.15 X 10^{-4}	1.16	0.12	4.50

Notes:

1) The uncertainty in the ϕ_{Bn} data is 0.01 eV except for $\phi_{Bn}{}^{I-V}$ for Pt and Ni where the uncertainty is 0.02 eV.

2) (kT/q) = 0.0255 eV at 295.5 K.

3) All measurements were made on 7.01 X 10^{-5} cm^2 diodes.

4) $\Delta\phi_{Bn} = \phi_{Bn}{}^{C-V} - \phi_{Bn}{}^{I-V}$.

5) ϕ_{metal} data were obtained from Ref. 32.

Assuming that a metal-semiconductor contact on a cleaned n-type semiconductor surface has an interfacial layer which is thin enough to be transparent to electrons and also assuming that the surface state density at the metal-semiconductor interface is an exclusive property of the semiconductor, the dependence of Schottky barrier height upon metal work function (ϕ_m) may be modelled as follows[32,33]

$$\phi_{Bn} = c_2 \cdot \phi_m + c_3 \tag{14}$$

The constant c_2 is related to the surface state density D_s by[32]

$$D_s \simeq 1.1 \;\; X \;\; 10^{13} \cdot \frac{(1 - c_2)}{c_2} \tag{15}$$

A plot of ${\phi_{Bn}}^{C-V}$ versus ϕ_m is shown in Fig. VII and a least squares fit of these data gives

$$\phi_{Bn} = 0.194 \cdot \phi_m - 0.183 \tag{16}$$

The degree of fit between Eq. (14) and a straight line is 0.95. By using $c_2 = 0.194$ in Eq. (4) the surface state density of MBE grown n-type (111)A GaAs is estimated to be 4.57 X 10^{13} $\pm$ 1.14 X 10^{12} $cm^{-2} \cdot eV^{-1}$. Since ${\phi_{Bn}}^{C-V}$ data is not affected by image force effects, and therefore more closely represents the true barrier height than the ${\phi_{Bn}}^{I-V}$ data, it has been used in deriving Eq. (16).

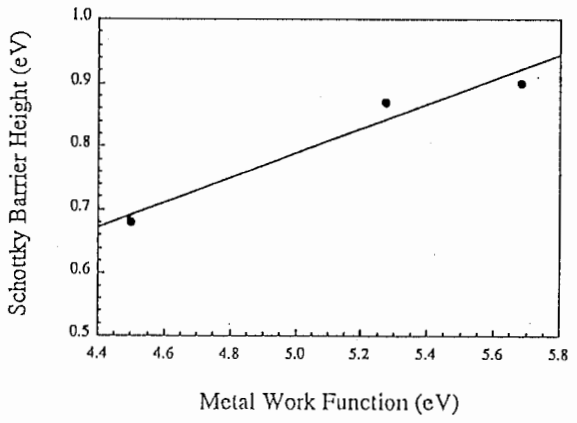

Fig. 7 - Schottky barrier height versus metal work function for Pt, Ni and Cr on n-type (111)A GaAs, measured at 295.5 K.

A D_s value of 6.5 X 10^{13} $cm^{-2} \cdot eV^{-1}$ has been reported for VPE (100) GaAs[34]. The

uncertainty in this value is calculated to be ± 2.60 X 10^{12} $cm^{-2}{\cdot}eV^{-1}$. By applying Eq. (14) to the ${\phi_{Bn}}^{C-V}$ data reported in Ref. 35 for Ni, Cr and Bi on LEC (100) GaAs a D_s value of 7.15 X 10^{13} ± 7.5 X 10^{11} $cm^{-2}{\cdot}eV^{-1}$ is calculated. Ref. 35 contains Schottky barrier height data for several metals. Eq. (14) has been applied to three points from this data which cover the widest range of metal work functions and which also correspond to the metals studied on (111)A GaAs. A D_s value of 1.25 ± 1.0 X 10^{14} $cm^{-2}{\cdot}eV^{-1}$ has been reported for (110) GaAs[33]. The estimate of D_s for (111)A GaAs is lower than D_s values of GaAs surfaces which contain arsenic and this implies that Schottky barrier heights on (111)A GaAs show a stronger dependence on metal work function and are less influenced by Fermi level pinning than Schottky barriers on GaAs surfaces that contain arsenic.

The constants c_2 and c_3 of Eq. (14) are related to the surface energy level (ϕ_0) by[32)]

$$\phi_0 = \frac{E_g}{q} - \frac{c_2\chi + c_3 + \Delta\phi}{1 - c_2} \tag{17}$$

E_g is the semiconductor band gap (1.42 eV for GaAs at 295.5 K), χ is the electron affinity of the semiconductor (4.07 for GaAs[32,33)]) and $\Delta\phi$ represents barrier lowering due to image force effects. By substituting $c_2 = 0.194$, $c_3 = -0.183$ plus the $\Delta\phi_{Bn}$ data from Table VII into Eq. (17), $q\phi_0 = 0.47 \pm 0.10$ eV is observed for (111)A GaAs. For Refs. 34, 35 and 33: $q\phi_0$ equals 0.43 ± 0.10 eV, 0.46 ± 0.08 eV and 0.53 ± 0.33 eV respectively. The surface energy level of n-type (111)A GaAs is similar to that of n-type (100) GaAs and lower than the $q\phi_0$ value for (110) GaAs which is presented in Ref. 33.

The ideality factors in Table VII were calculated using[32)]

$$n = \frac{q}{kT}\frac{\Delta V}{\Delta \ln J_s} \tag{18}$$

They are higher than 1.02 - 1.04, which correspond to "ideal" metal contacts on n-type GaAs. In addition, they are higher than the previously reported n value of 1.06 for Ti/Au Schottky contacts on p-type MBE grown (111)A GaAs, which were also fabricated using a dilute H_3PO_4 cleaning process prior to Schottky metal deposition[36]. The contacts discussed in this letter were deposited into recesses unlike the Ti/Au contacts on p-type (111)A GaAs described in Ref. 36. It is believed that the HF based recess etch introduced microscopic roughness on the surface of the n^- layer onto which the Schottky contacts were deposited. This appears to have caused

physical disruptions in the metal-semiconductor interface which has resulted in high ideality factors.

Surface roughness introduced by recess etching is not believed to have influenced the values of D_s and $q\phi_0$. These parameters are determined by the chemistry of the (111)A surface. Since the Schottky diodes were fabricated on epitaxial GaAs which was grown on a (111)A GaAs substrate which is misoriented by 5° toward [100], the D_s and $q\phi_0$ values have been measured on a surface which contains microsteps[31] and is not truly planar. The main observation from our data is that the surface state density of a gallium terminated, non-planar GaAs surface is lower than the surface state density of planar GaAs surfaces that contain arsenic. This is explained by differences in surface chemistry which lead to differences in reactivity between GaAs and metal overlayers.

In conclusion, we have measured the Schottky barrier heights of Pt, Ni and Cr on Si doped *n*-type GaAs grown by MBE on a (111)A GaAs substrate which is misoriented by 5° toward [100]. By fitting a straight line to a plot of Schottky barrier height versus metal work function we have estimated that the surface state density of the *n*-type epi-layer is 4.57 X 10^{13} $cm^{-2}{\cdot}eV^{-1}$. This is lower than D_s values for the (100) and (110) GaAs surfaces implying that the dependence of Schottky barrier heights upon metal work functions is stronger on (111)A GaAs than on surfaces which contain arsenic atoms.

Experiments similar to those described above and in the previous section have been done with Ti/Au contacts on n-type GaAs. Table VIII contains data from 3 comparison experiments.

Table VIII Properties of Schottky Contacts on n^+/n^- GaAs.

Sample	$\phi_{Bn}{}^{I-V}$	n	$\phi_{Bn}{}^{C-V}$	V_{Bi}	$\Delta\phi_{Bn}$
	eV		eV	V	eV
1)Ti/Au/HCl/(111)A	0.60	1.10	0.78	0.77	0.18
1)Ti/Au/HCl/(100)	0.63	1.11	0.84	0.83	0.21
2)Ti/Au/H_2SO_4/(111)A	0.58	1.12	0.74	0.74	0.16
2)Ti/Au/H_2SO_4/(100)	0.64	1.13	0.82	0.81	0.18

3)Au on (111)A	0.67	1.86	–	–	–
3)Au on (100)	0.73	2.74	–	–	–

In table VIII, the samples are identified by the type of Schottky metal, the surface cleaning reagent and the GaAs surface on which the contacts were depositied. The barrier heights of Ti/Au contacts on n-type (100) are higher than the barrier heights of equivalent Ti/Au contacts on (111)A 5° to [100]. The Schottky relation for metals on GaAs predicts that the barrier height fo Ti on n-type GaAs should be about 0.23 eV. Therefore the barrier height of Ti on n-type (111)A GaAs is closer to the ideal Schottky relation than the barrier height of Ti on n-type (100) GaAs. This may be explained by the same argument which was used for Ti/Au on p-type GaAs. (111)A GaAs is Ga terminated. Ga surface atoms do not have extra electrons which can react with metals. (100) GaAs has a mixture of Ga and As atoms at the surface. Since As surface atoms have an unshared pair of electrons they can react with metal overlayers. Chemical reactions between As surface atoms and metal overlayers form compounds which can distort the thermionic emission process.

The ideality factors in tables VIII appear to have been influenced by the HF based recess etch which was used in the diode fabrication process. This is similar to the data presented in table VII.

By adding the C-V barrier heights for Cr and Ni on both n-type and p-type GaAs, presented in tables VI and VII and by adding the same data for Ti, presented in tables V and VIII we observe that the following relation is observed.

$$E_g = \phi_{Bn} + \phi_{Bp} \tag{19}$$

Using Cr and Ni data obtained from H_3PO_4 cleaned (111)A GaAs and using Ti data from H_2SO_4 cleaned (111)A GaAs:

Ni - $\phi_{Bn} + \phi_{Bp} = 0.87$ eV + 0.57 eV = 1.44 eV

Cr - $\phi_{Bn} + \phi_{Bp} = 0.68$ eV + 0.70 eV = 1.38 eV

Ti - $\phi_{Bn} + \phi_{Bp} = 0.74$ eV + 0.72 eV = 1.46 eV

E_g for GaAs is 1.42 eV at 295.5K, the temperature at which all of my I-V and C-V measurements have been made. Within experimental error eq. 19 is observed to be true for Ni, Cr and Ti on (111)A GaAs.

3) Field Effect Transistors on (111)A GaAs.

Once working ohmic and Schottky contacts can be fabricated the, properties of working devices may be studied. A full description of FETs appears in "Physics of Semiconductor Devices" by S.M. Sze. General aspects of FETs are not discussed in this report.

Several attempts have been made to fabricate simple FETs on n-type and p-type (111)A GaAs and compare their d.c. properties to those of FETs on (100) GaAs. While it has been possible to make FETs which modulate channel current, current saturation has not been achieved. The surface morphology of epitaxial GaAs on p-type (111)A GaAs and on n-type (111)A 5° towards (100) GaAs is smooth enough to successfully form Schottky contacts. Undoped buffer layers, which have not yet been demonstrated on (111)A FET structures grown at ATR, are necessary for high performance FETs. All FETs discussed in thos report are recessed gate FETs where the ohmic contacts are situated on a high doped epitaxial layer (p^+ or $n^+ \simeq 3$ - 5 X 10^{18} cm^{-3}) and the gate contacts are situated on a low doped epitaxial layer (p^- or $n^- \simeq 2$ - 3 X 10^{17} cm^{-3}). In addiition, the gate metal used for all of these studies was Ti(100 Å)/Au(2000 Å).

3.1) FETs on P-type (111)A GaAs.

FETs with Ti/Au gates and Mn/Au ohmic contacts have been studied in detail. Since the all the experimental results are similar only a few data will be discussed in detail.

FETs have been constructed by first using mesa etching to isolate individual devices. Au/Mn ohmic contacts were deposited as outlined in appendix 1 of this report. Ti/Au Schottky contacts were subsequently deposited as described in appendix 1 of this report. A plot of drain current versus gate voltage is shown in Fig. 8. For voltages greater than -0.25 volts the drain current is zero, or the device is off. For voltages lower than -0.25 volts the drain current gradually increases and the device is on. For gate voltages above the threshold voltage, the transconductance (g_m) of the device increases up to a maximum value. There are two problems with these data.

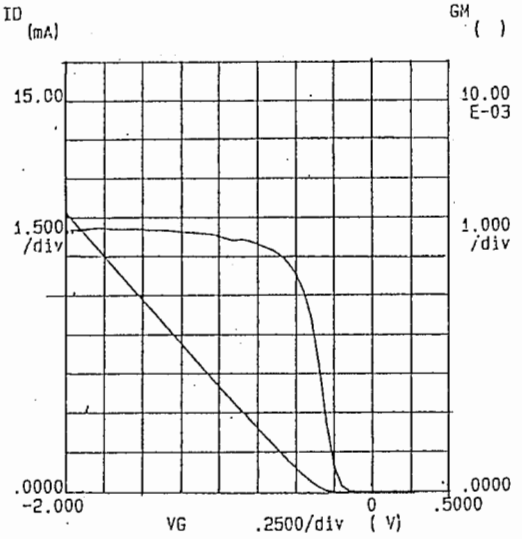

Fig. 8 Drain current and transconductance versus gate voltage for a 3 μm X 275 μm FET on p-type (111)A GaAs.

First, the drain current is positive. This suggests that the electron current is being measured. For FETs on p-type GaAs drain current should be negative, since the carriers are holes. The second problem is that the gain is extremely low. The peak gain is about 2 mS/mm. The g_m of FETs on p-type GaAs should be near 21 mS/mm. A plot of drain current versus source drain voltage is shown in Fig. 9. For voltages greater than 0 volts, the channel current is modulated by the application of a gate voltage.

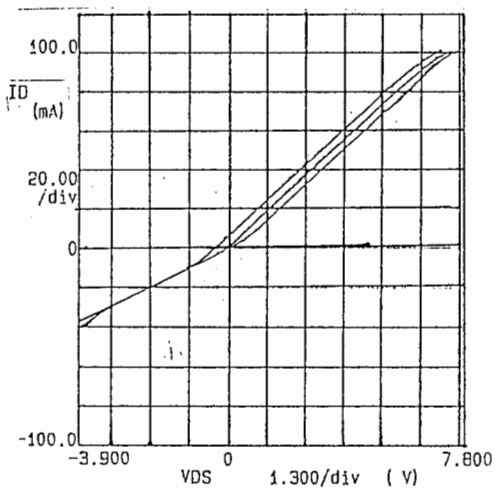

Fig. 9 Drain current versus source drain voltage for a 3 μm X 270 μm FET on p-type (111)A GaAs.

As in Fig. 8 the switching is observed where the drain current is positive. For FETs on p-type GaAs, switching should be observed for negative drain currents.

Also, above 0 volts the drain current never saturates. The drain current should saturate provided that there is not an alternative current path beneath the gate.

These particular results come from devices where the Si doped active layer sits on a buffer layer. Similar results have been obtained from FETs where the active layer sits on the S.I. (111)A and (100) GaAs substrates. These problems have been observed for identical devices on both p-type (111)A and p-type (100) GaAs. FETs with several recess depths have been studied and pinchoff voltage (V_p) is virtually independent of channel depth, indicating that current leakage is a problem. We know that the buffer layers grown in ATR's Varian MBE system are slightly p-type.

3.2) FETs on N-type (111)A GaAs Misoriented by 5° toward [100] GaAs.

Most of the problems discussed in the previous section also apply to FETs which have been fabricated on n-type (111)A GaAs. Fig. 10 contains a plot of drain current and transconductance versus gate voltage for FETs with gate contacts consisting of Ti/Au which has been deposited into a recess which was cleaned with H_2SO_4 before Schottky metal deposition. The drain current turns on around -5.8 volts and the transconductance peaks at about -9.8 volts. The peak g_m is about 5mS/mm and this is extremely low. The correct polarity is observed for both drain current and g_m which indicates that an electron current is flowing in these devices. These data indicate that the channel layer is very thick and that current leakage is occuring.

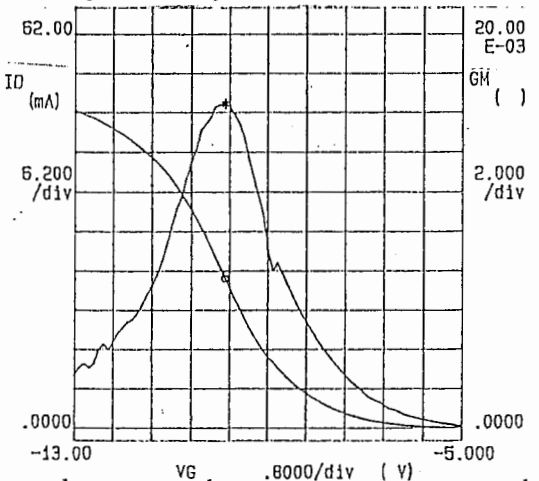

Fig. 10. Drain current and transconductance versus gate voltage for 3μm X 275 μm FETs on n-type (111)A GaAs.

Fig. 11 contains a plot of drain current versus drain-source voltage. Since current saturation is not observed for relatively low voltages, it appears that current is

leaking from the channel, most likely into the substrate. As mentioned in section 3.1, the buffer layers in these devices are slightly p-type. In the case of n-type FETs this can serve to enhance current confinement in the channel region, provided that an external bias is applied to the buried p-type layer. When no external bias is applied to this layer, as is the case here, it can accentuate current leakage[37].

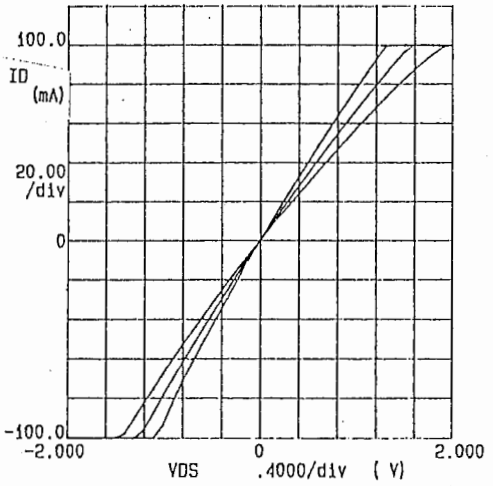

Fig. 11 Drain current versus drain source voltage for 3μm X 275 μm FETs on n-type (111)A GaAs.

Eventhough the n^-layer was recessed before Schottky metal deposition the channel thickness is still excessively high. This indicates that the actual channel depth of these devices may be the sum of the grown channel layer plus part of the buffer layer. FETs with different recess depths have been studied and V_p has been found to be virtually independent of channel thickness.

4) Conclusions

1. Low resistance Ni/AuGe/Au contacts have been demonstrated on Si-doped n-type (111)A epitaxial GaAs.

2. Differences in the surface chemistry of n-type MBE epi-layers grown on (111)A and (100) GaAs have no affect on the contact resistance of Ni/AuGe/Au ohmic contacts.

3. Low resistance Mn/Au ohmic contacts have been demonstrated on Si doped p-type (111)A epitaxial GaAs.

4. Differences in the surface chemistry between (111)A GaAs and (100) GaAs affect the properties of Schottky contacts on these surfaces.

5. The surface state density of (111)A GaAs is lower than the surface state density of (100) GaAs.

6. The general relation $E_g = \phi_{Bn} + \phi_{Bp}$ applies to (111)A GaAs.

5) Suggested Possibilities for Extending the Projects Discussed in this Report.

1) Field Effect Transistors.

Eventhough functional Schottky and ohmic contacts have been demonstrated on n-type and p-type (111)A GaAs high performance field effect transistors have yet to be successfully fabricated on this material. The problems have been outlined in section 3 and the following recommendations will hopefully lead to solutions.

1. Maximum transconductance of a FET needs to be measured on devices which have short gate lengths, typically about 1 to 1.2 μm. The shortest gate length on ATR's mask set is $\simeq 3\mu$m. It would be helpful if a new mask set, containing FETs with shorter gate lengths, could be designed and used by the materials group.

2. The interface at the bottom of the channel epitaxial layer needs to be controlled more precisely in order to eliminate current leakage from FET channels into the substrates on which the epi-layers are grown. This may be most easily achieved by developing a process to grow high quality undoped buffer layers which separate the device channels from the substrates.

2) Ohmic Contacts.

3. A good comparison between the diffusion of zinc and manganese in p-type ohmic contacts on GaAs does not appear to have been written. This would be very interesting to study. It would require extensive secondary ion mass spectroscopy analysis (SIMS) as well as a lot of device processing and electrical testing. I think that ATR is in a position to do this type of work and it would benefit everyone in the GaAs community.

4. In order to accurately determine the specific contact resistivity of ohmic contacts current - voltage data from a Kelvin resistor is required. Since there are no Kelvin resistor patterns on ATR's mask sets it would be helpful if this type of test structure could be designed in to any new mask sets.

3) Schottky Contacts

My work has focussed on studying the Schottky properties of Ti, Pt, Cr and Ni on n-type and p-type (111)A GaAs. I encourage other researchers at ATR to continue to study these metals as well as the properties Schottky contacts based on other metals or combinations of metals.

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Appendix 1 Process Flow Used for Fabrication of Ohmic Contacts, Schottky Diodes and Discreet Field Effect Transistors.

Part 1 Device Isolation.

1. Place the sample in a beaker of acetone situated in the ultrasonic bath for 3 minutes. This degreases the GaAs surface.

2. Rinse the sample in methanol for 1 minute. This removes acetone from the GaAs surface.

3. Rinse the sample in flowing deionized (D.I.) H_2O for 3 minutes. This removes the methanol from the GaAs surface.

4. Dry the sample with N_2.

5. Place the sample in 10:1 D.I. H_2O : NH_4OH for 5 seconds and then rinse it in flowing D.I. H_2O for 3 minutes. This removes any native arsenic oxide and replaces it with gallium oxide.

6. Rinse the sample in flowing D.I. H_2O for 3 minutes.

7. Dry the sample with N_2.

8. Bake the GaAs for 30 minutes at 120°C. This removes any residual H_2O from the GaAs surface.

9. Coat the GaAs surface with photoresist. Put the GaAs on the chuck of the manual spinner and make sure that the vacuum pump is turned on. Use the equivalent of 3 cm^3 (per 2 inch dia. wafer) of a 3:1 AZ 1350J resist:AZ thinner mixture. Set the first spin cycle at 500 rpm for 10 seconds and the second spin cycle at 5000 rpm for 40 seconds. Apply the resist to the GaAs surface during the first spin cycle. This process gives a photoresist coating which is about 1 μm thick.

10. Bake the sample for 25 minutes at 85°C. This "softbake" removes solvents from the photoresist.

11. Expose the photoresist with mask #2, of the triangle pattern mask set, using the Canon PLA500 aligner. Set the exposure integral to 10 and use proximity mode.

12. Develop the sample in 0.5:1 AZ developer : H_2O for 1 minute.

13. Rinse the sample in flowing D.I. H_2O for 3 minutes and dry the sample with N_2.

14. Bake the sample for 20 minutes at 120° C. This "hardbake" stengthens the resist so that it can withstand etching.

15. Etch the samples in $HF(46\%):H_2O_2(35\%):H_2O$ = 2:16:100. At room temperature, the etch rate for (111)A GaAs is about 0.48 μm/min and the etch rate for (100) GaAs is about 1.02 μm/min.

16. Rinse the sample in flowing D.I. H_2O for 3 minutes and dry with N_2.

17. Strip the resist by placing the sample in acetone for 1 minute.

18. Rinse the sample in methanol for 1 minute.

19. Rinse the sample in flowing D.I. H_2O for 3 minutes and dry the sample with N_2.

20. Check the mesa height with the Dektak surface profilometer.

21. Store the sample in a N_2 ambient.

Part 2 Ohmic Contact Formation

1. Place the sample in 10:1 D.I. H_2O : NH_4OH for 5 seconds and rinse in flowing D.I. H_2O for 3 minutes. This removes any native arsenic oxide and replaces it with gallium oxide.

2. Rinse the sample in flowing D.I. H_2O for 3 minutes.

3. Dry the sample with N_2.

4. Bake the GaAs for 30 minutes at 120°C. This removes any residual H_2O from the GaAs surface.

5. Coat the GaAs surface with photoresist. Put the GaAs on the chuck of the manual spinner and make sure that the vacuum pump is turned on. Use the equivalent of 3 cm^3 (per 2 inch dia. wafer) of a 3:1 AZ 1350J resist:AZ thinner mixture. Set the first spin cycle at 500 rpm for 10 seconds and the second spin cycle at 5000 rpm for 40 seconds. Apply the resist to the GaAs surface during the first spin cycle. This process gives a photoresist coating which is about 1 μm thick.

6. Bake the sample for 25 minutes at 85°C. This "softbake" removes solvents from the photoresist.

7. Place the sample in chlorobenzene for 15 minutes at room temperature.

8. Dry the sample with N_2 and bake the sample at 85°C for 10 minutes.

9. Expose the photoresist with mask #3, of the triangle pattern mask set, using the Canon PLA500 aligner. Set the exposure integral to 20 and use proximity mode.

10. Develop the sample in 2:1 AZ developer : H_2O for 1 minute.

11. Bake the sample for 20 minutes at 120° C.

12. Clean the samples with a 20:1 solution of H_2O : acid for 5 to 10 seconds. The particular acid and the cleaning time may be chosen by the researcher.

13. Rinse the sample in flowing D.I. H_2O for 3 minutes. Dry the sample by placing spinning it on the manual spinner at 3000 rpm for 1 minute.

14. Load the sample along with the desired metals into the Anelva EVC 400B evaporator. For Ni/AuGe/Au contacts, pre-weigh 0.07 grams of Ni and 0.44 grams of a AuGe eutectic alloy and place them in the same boat. Pump the evaporator down to base pressure for at least 2 hours before depositing ohmic contact metal.

15. To form Ni/AuGe/Au contacts on n-type GaAs, deposit Ni and AuGe simultaneously. Be certain that all of this metal is deposited onto the GaAs so that the AuGe eutectic composition is preserved. The actual depositon conditions may be determined by the researcher. I operate the evaporator in manual

mode and initially ramp up the power from 0 % to 18 % at 2 %/min. I let the system idle at 18 % until the metal in the boat has melted. I then ramp the power up to 22 % in about 1 minute and then open the shutter to begin deposition. The power may then be adjusted to set the deposition rate. I deposit Ni/AuGe at about 1 Å/sec. After Ni/AuGe has been deposited, close the shutter and reduce the power to zero. Turn off the power supplies and switch the boat number so that the high current power supply is connected to the boat containing Au. Repeat the deposition process until the desired amount of Au has been deposited.

16. To form Mn/Au contacts on p-type GaAs, I use the evaporator in manual mode and ramp the power from 0 % to 18 % at 2%/min. I let the system idle at 18% until the Mn has melted. I then open the shutter and deposit the desired quantity of Mn. I deposit Mn at a rate of 1 Å/sec. After connecting the high current power supply to the boat which contains Au, I deposit Au at 10 Å/sec.

17. After the metal deposition has been completed leave the system under vacuum for 15 minutes after the power supplies have been turned off.

18. Vent the system and remove the samples.

19. To perform metal lift off, place the sample in a beaker of acetone and place the beaker in the ultrasonic bath. Leave the sample in acetone until metal liftoff is complete.

20. Rinse the sample in methanol for 1 minute.

21. Rinse the sample in flowing D.I. H_2O for 3 minutes.

22. Dry the sample with N_2.

23. Store the sample in a N_2 ambient.

Part 3 Schottky Contact Formation

1. Place the sample In 10:1 D.I. H_2O : NH_4OH for 5 seconds and rinse in flowing D.I. H_2O for 3 minutes. This removes any native arsenic oxide and replaces it with gallium oxide.

2. Rinse the sample in flowing D.I. H_2O for 3 minutes.

3. Dry the sample with N_2.

4. Bake the GaAs for 30 minutes at 120°C. This removes any residual H_2O from the GaAs surface.

5. Coat the GaAs surface with photoresist. Put the GaAs on the chuck of the manual spinner and make sure that the vacuum pump is turned on. Use the equivalent of 3 cm^3 (per 2 inch dia. wafer) of a 3:1 AZ 1350J resist:AZ thinner mixture. Set the first spin cycle at 500 rpm for 10 seconds and the second spin cycle at 5000 rpm for 40 seconds. Apply the resist to the GaAs surface during the first spin cycle. This process gives a photoresist coating which is about 1 μm thick.

6. Bake the sample for 25 minutes at 85°C. This "softbake" removes solvents from the photoresist.

7. Place the sample in chlorobenzene for 15 minutes at room temperature.

8. Dry the sample with N_2 and bake the sample at 85°C for 10 minutes.

9. Expose the photoresist with mask #4, of the triangle pattern mask set, using the Canon PLA500 aligner. Set the exposure integral to 20 and use proximity mode.

10. Develop the sample in 2:1 AZ developer : H_2O for 1 minute.

11. Bake the sample for 20 minutes at 120° C.

12. Clean the samples with a 20:1 solution of H_2O : acid for 5 to 10 seconds. The particular acid and the cleaning time may be chosen by the researcher.

13. Rinse the sample in flowing D.I. H_2O for 3 minutes. Dry the sample by placing spinning it on the manual spinner at 3000 rpm for 1 minute.

14. Load the sample along with the desired metals into the Anelva EVC 400 evaporator and pump the system for at least 16 hours.

15. For Schottky metal deposition I operate the evaporator in manual mode and initially ramp up the power from 0 % to 18 % at 2 %/min. I let the system idle at 18 % until the metal in the boat has melted. I then ramp the power up to 22 % in about 1 minute and then open the shutter to begin deposition. The power may then be adjusted to set the deposition rate. My Schottky metal experiments have focussed on forming Schottky barriers consisting of a thin metal layers covered with thicker layers of Au. I deposit the first metal layer at a rate of 1 Å/sec and after the desired amount of metal has been deposited I close the shutter and reduce the power to zero. Turn off the power supplies and switch the boat number so that the high current power supply is connected to the boat containing Au. Repeat the deposition process until the desired amount of Au has been deposited.

16. After the metal deposition has been completed leave the system under vacuum for 15 minutes after the power supplies have been turned off.

17. Vent the system and remove the samples.

18. To perform metal lift off, place the sample in a beaker of acetone and place the beaker in the ultrasonic bath. Leave the sample in acetone until metal liftoff is complete.

19. Rinse the sample in methanol for 1 minute.

20. Rinse the sample in flowing D.I. H_2O for 3 minutes.

21. Dry the sample with N_2.

Appendix 2 Calculation of Mn weight percentage in Mn/Au ohmic contacts.

The weight percentage of Mn may be calculated as follows.
Eventhough the volumes of Au and Mn in these contacts are different, the surface area of Au and Mn are the same. Therefore, the weight of each metal is proportional to the density multiplied by the thickness.

$\rho_{Au} = 19.3$ g/cm^3 $\qquad$ $\rho_{Mn} = 7.43$ g/cm^3

$T_{Au} = 2154$ Å $\qquad$ $T_{Mn} = 221$ Å

weight = thickness × density × area

weight$_{Au}$ = (2154 Å) (19.3 g/cm^3) (10^{-4}cm/Å) (area) = 4.157 g/cm^2 (area)

weight$_{Mn}$ = (221 Å) (7.43 g/cm^{-3}) (10^{-4}cm/Å) (area) = 0.164 g/cm^2 (area)

weight % Mn = $\frac{weight_{Mn}}{weight_{total}} \times 100 = \frac{0.164(area)}{4.321(area)} = 3.80$

Appendix 3 Alloy furnace Temperature Distribution

Figure 12 shows the distribution of temperature as a function of distance from the center of the Koyo Lindberg alloy furnace for a set point temperature of 370°C. The peak measured temperature at the center of the furnace is 399°C. The difference between the actual temperature and the set point temperature is about 30°C for temperatures between 350° and 450°C. The data in the graph were measured while the furnace contained an N_2 atmosphere. The N_2 pressure was 0.8 kg/cm^2 and the N_2 flow was 1.7 liters/min. The set point temperature for the 450°C alloy processes in my experiments has always been 420°C. The temperature of this furnace takes about 50 minutes to stabilize. Samples should be loaded into the quartz tube but positioned outside of the furnace for the first 50 minutes after the heating power has been turned on. The measured overshoot temperature is about 100°C higher than the set point temperature and this peak is reached at about the 12^{th} minute after the furnace has been turned on.

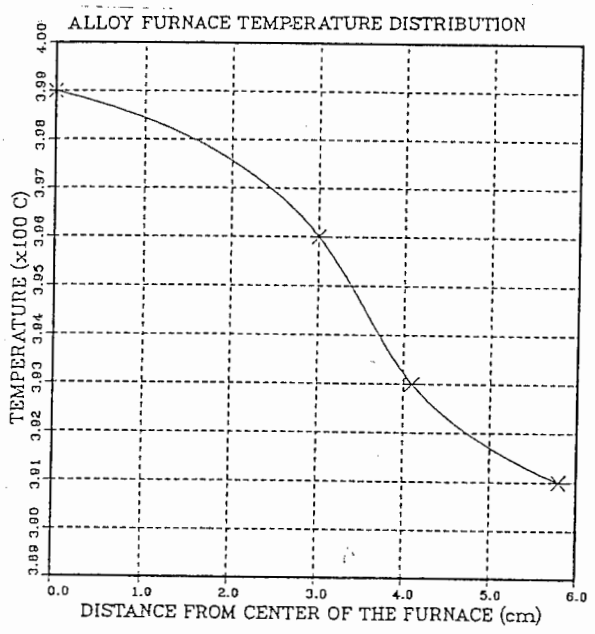


Fig. 12 - Real temperature versus distance from the center of the Koyo Lindberg alloy furnace for a set point temperature of 370°C.

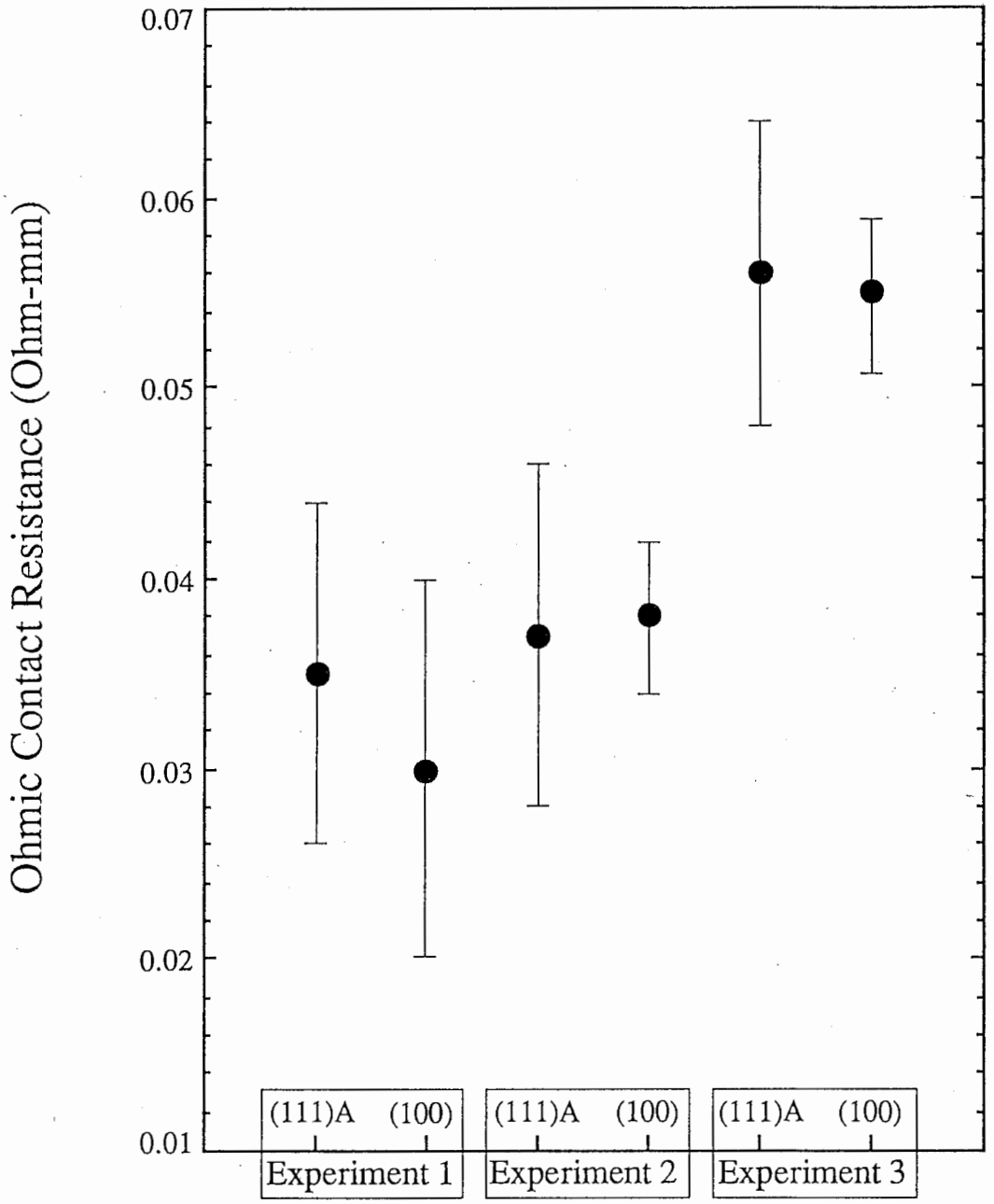

Ohmic Contact Resistance (Ohm-mm)
0.07
0.06
0.05
0.04
0.03
0.02
0.01
(111)A
(100)
(111)A
(100)
(111)A
(100)
Experiment 1
Experiment 2
Experiment 3

Fig 1

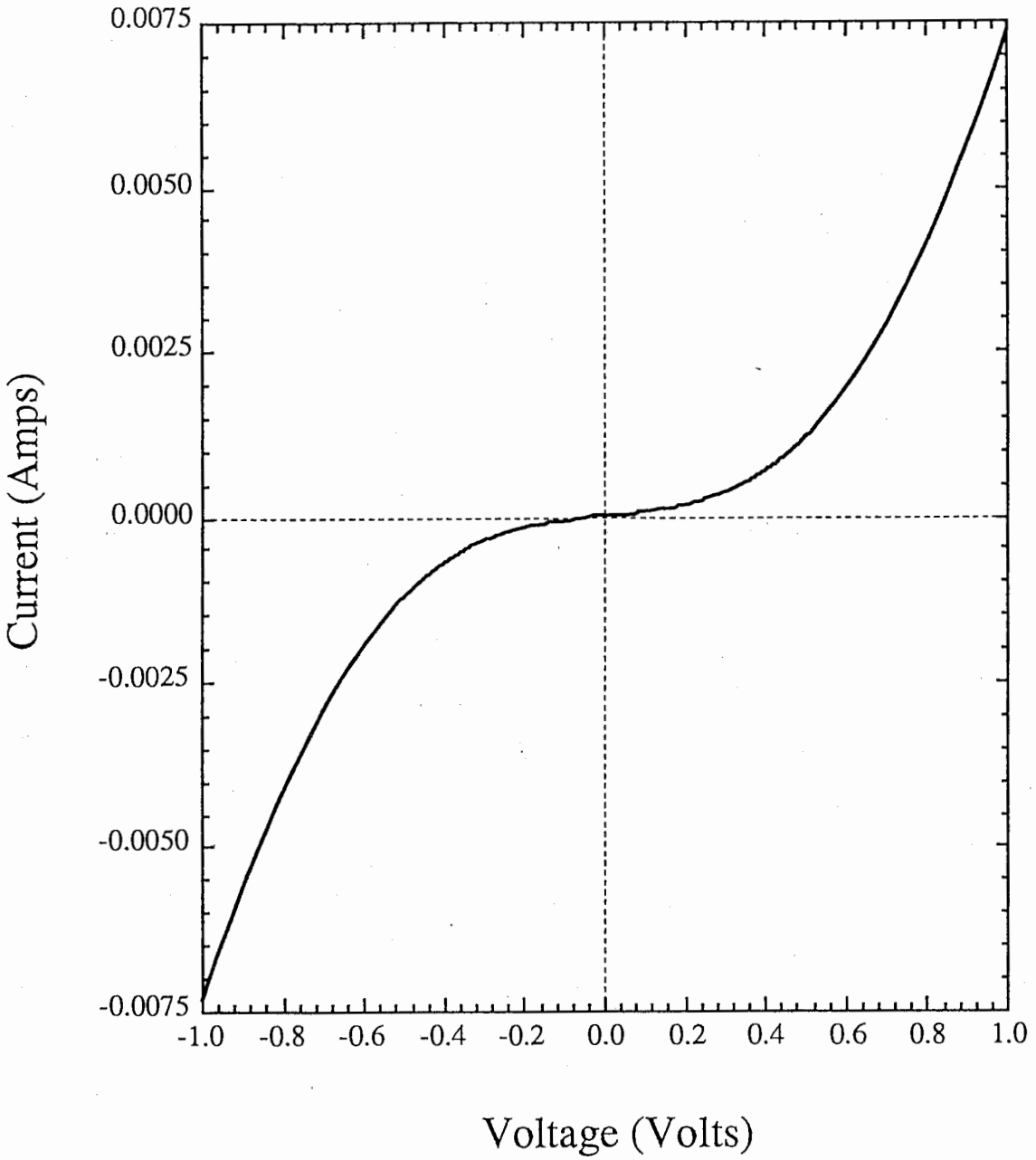
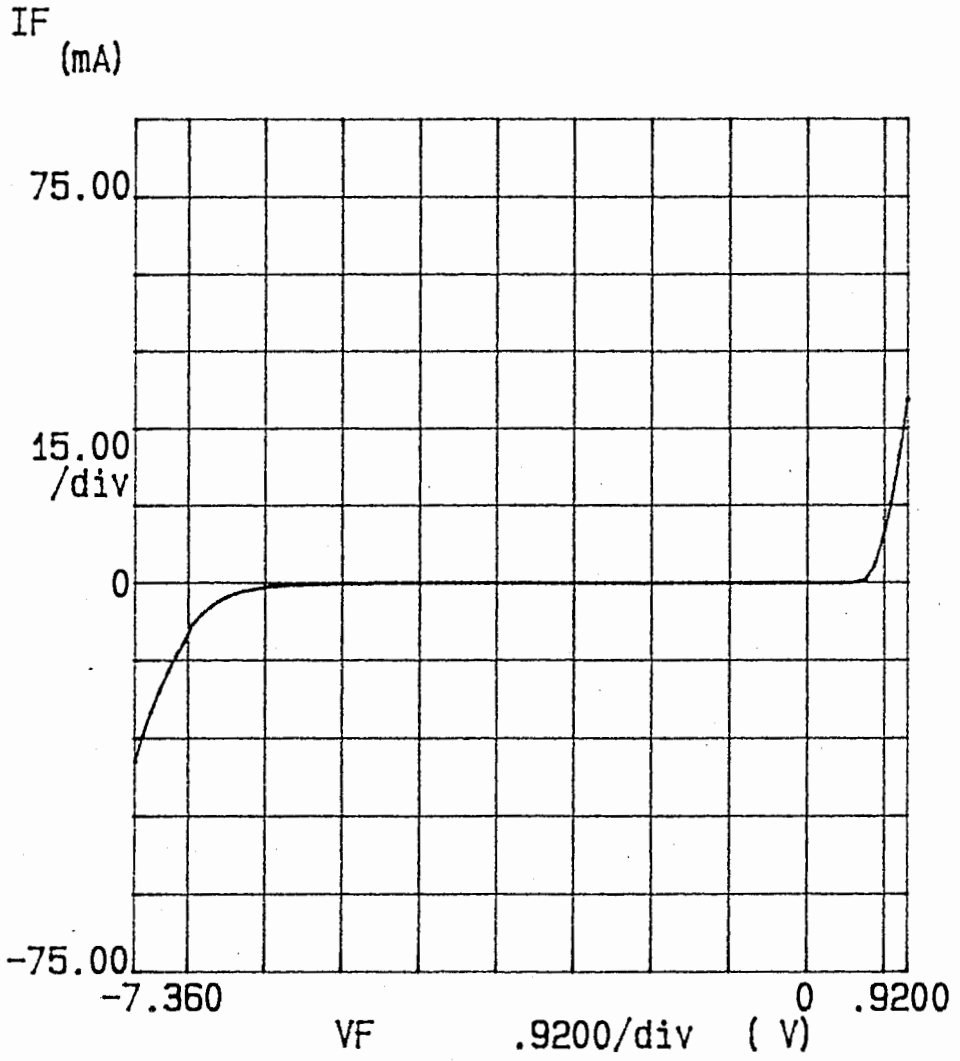

0.0075
0.0050
0.0025
0.0000
-0.0025
-0.0050
-0.0075
Current (Amps)
-1.0
-0.8
-0.6
-0.4
-0.2
0.0
0.2
0.4
0.6
0.8
1.0
Voltage (Volts)

Fig 2

****** GRAPHICS PLOT ******

NI/AU ON N-TYPE (111) A



Variable1:
VF -Ch1
Linear sweep
Start -8.0000V
Stop 1.2000V
Step .1000V

Constants:
V -Ch3 .0000V

Fig 3

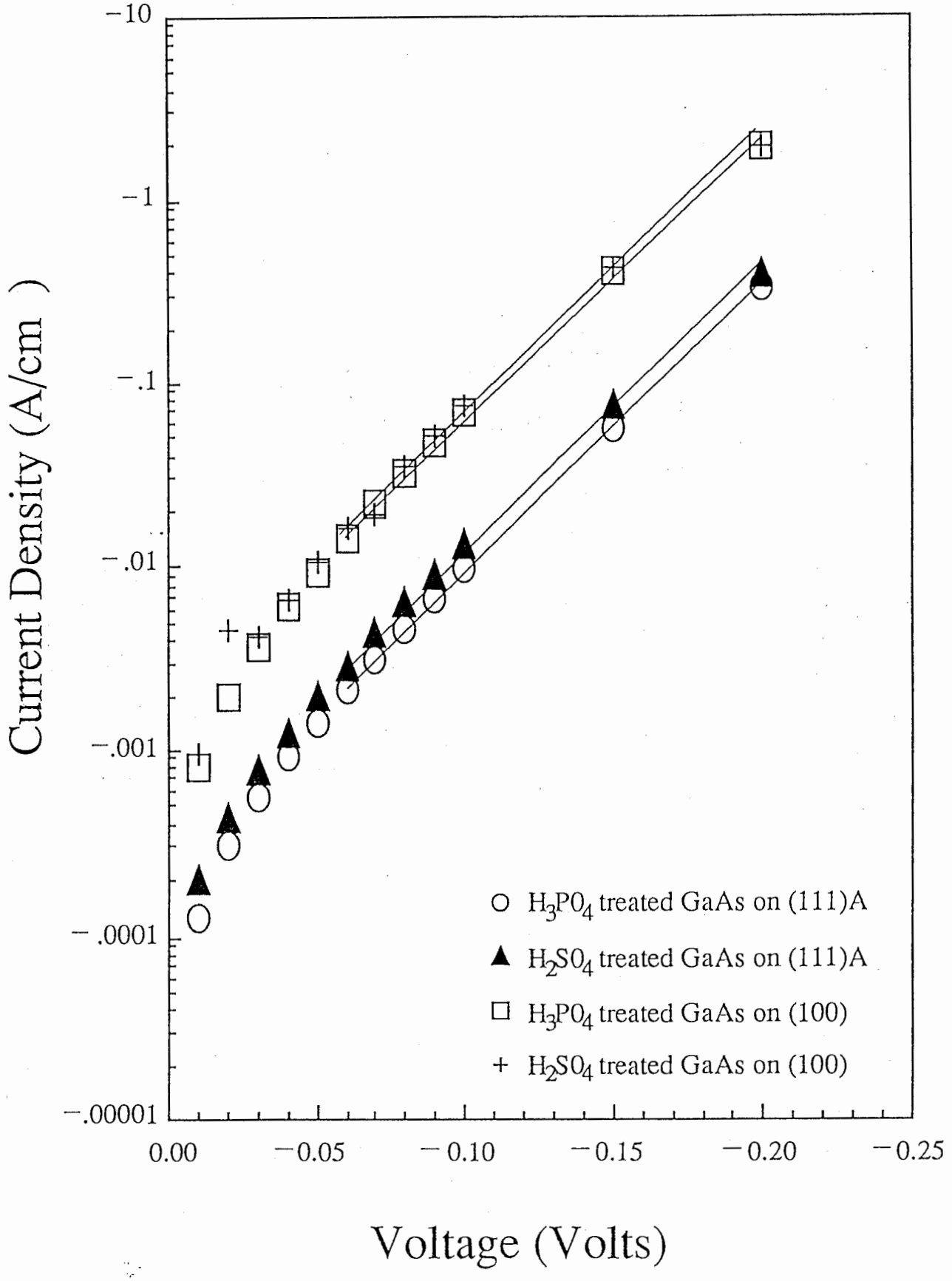

−10
−1
−.1
−.01
−.001
−.0001
−.00001
Current Density (A/cm)
0.00
−0.05
−0.10
−0.15
−0.20
−0.25
Voltage (Volts)
H3PO4 treated GaAs on (111)A
H2SO4 treated GaAs on (111)A
H3PO4 treated GaAs on (100)
H2SO4 treated GaAs on (100)

Fig 4

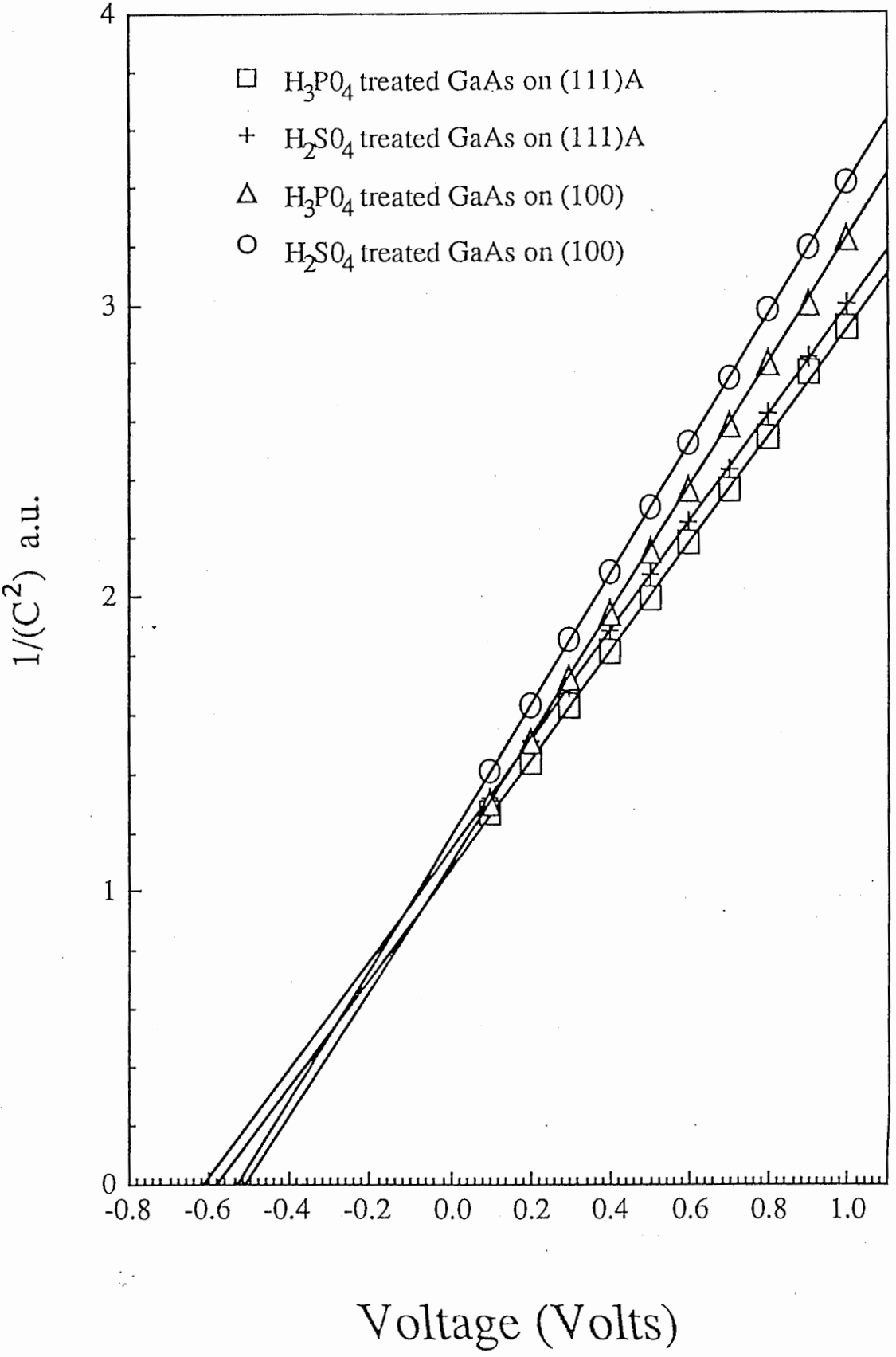

4
3
2
1
0
-0.8
-0.6
-0.4
-0.2
0.0
0.2
0.4
0.6
0.8
1.0
H_3P0_4 treated GaAs on (111)A
H_2S0_4 treated GaAs on (111)A
H_3P0_4 treated GaAs on (100)
H_2S0_4 treated GaAs on (100)
$1/(C^2)$ a.u.
Voltage (Volts)

Fig 5

Table V

	On (111)A GaAs		On (100) GaAs	
Characteristics of the p-type epitaxial layers.				
Carrier Concentration (cm^{-3})	2.85×10^{17} (Si)		3.65×10^{17} (Be)	
Carrier Mobility ($cm^2/Vsec$)	179		157	
Layer Thickness (μm)	0.5		1.6	
Electrical data from Ti/Au contacts on p-type epitaxial GaAs grown by MBE.				
Surface cleaning reagent	H_2SO_4	H_3PO_4	H_2SO_4	H_3PO_4
J_s (A/cm^2)	-4.52×10^{-4}	-2.69×10^{-4}	-2.23×10^{-3}	-1.96×10^{-3}
Ideality factor n	1.09	1.06	1.06	1.05
$\phi_{Bp}{}^{I-V}$ (eV)	0.61	0.62	0.56	0.56
V_i (V)	-0.61	-0.58	-0.53	-0.51
$\phi_{Bp}{}^{C-V}$ (eV)	0.72	0.69	0.61	0.59
$\Delta\phi_{Bp}$ ($\phi_{Bp}{}^{C-V} - \phi_{Bp}{}^{I-V}$) (eV)	0.11	0.07	0.05	0.03

Notes -

1) $\frac{kT}{q} = 0.0255$ eV at 295.5 K.
2) All measurements were made on $7.01 \times 10^{-5} cm^2$ diodes.
3) The uncertainty in ϕ_{Bp} values is 0.01 eV, except for $\phi_{Bp}{}^{I-V}$ on H_2SO_4 treated GaAs on (111)A GaAs. This uncertainty is 0.02 eV.
4) The uncertainty in the n values is 0.005 .

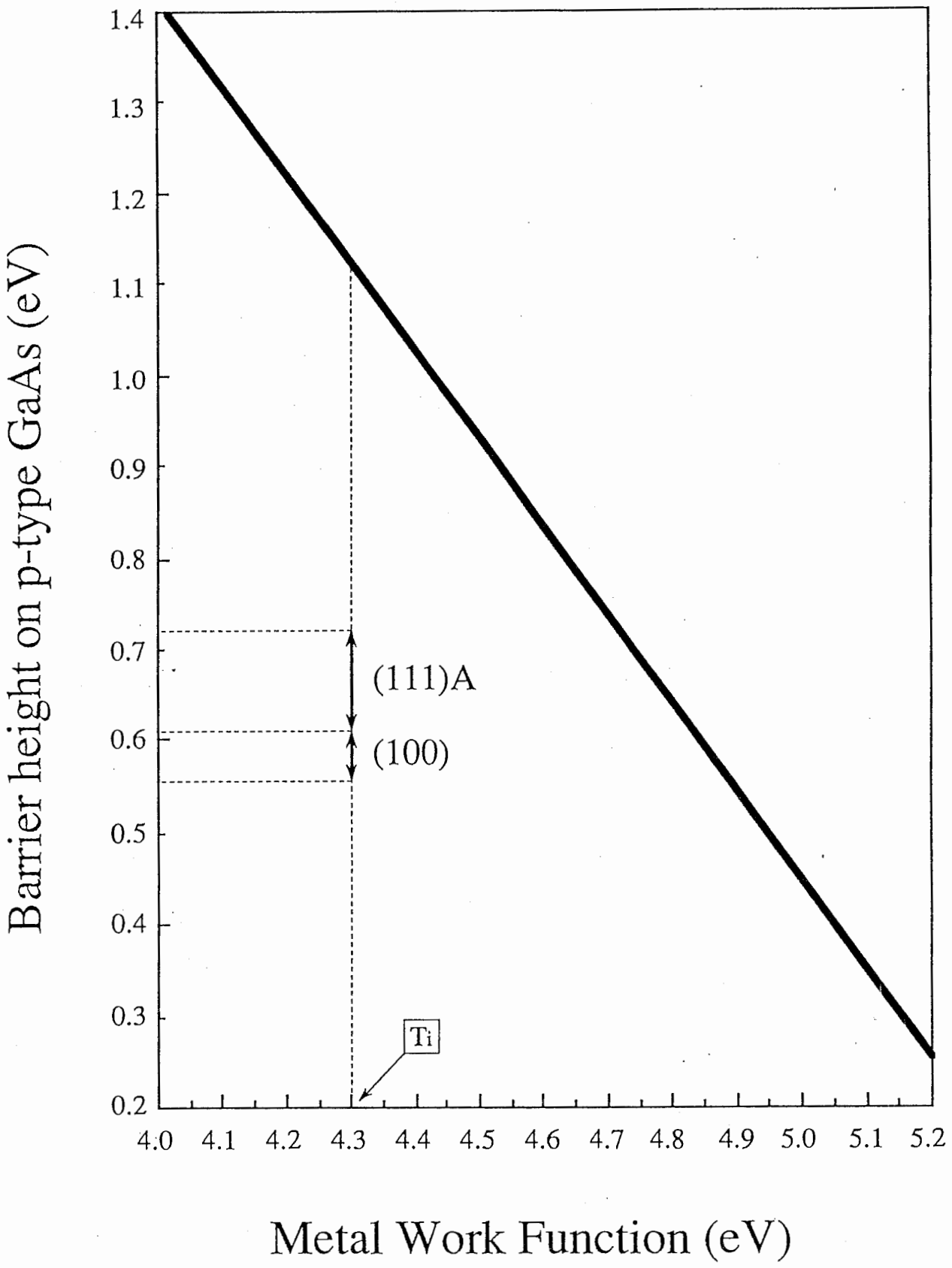

Barrier height on p-type GaAs (eV)
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
(111)A
(100)
Ti
4.0
4.1
4.2
4.3
4.4
4.5
4.6
4.7
4.8
4.9
5.0
5.1
5.2
Metal Work Function (eV)

Fig 6

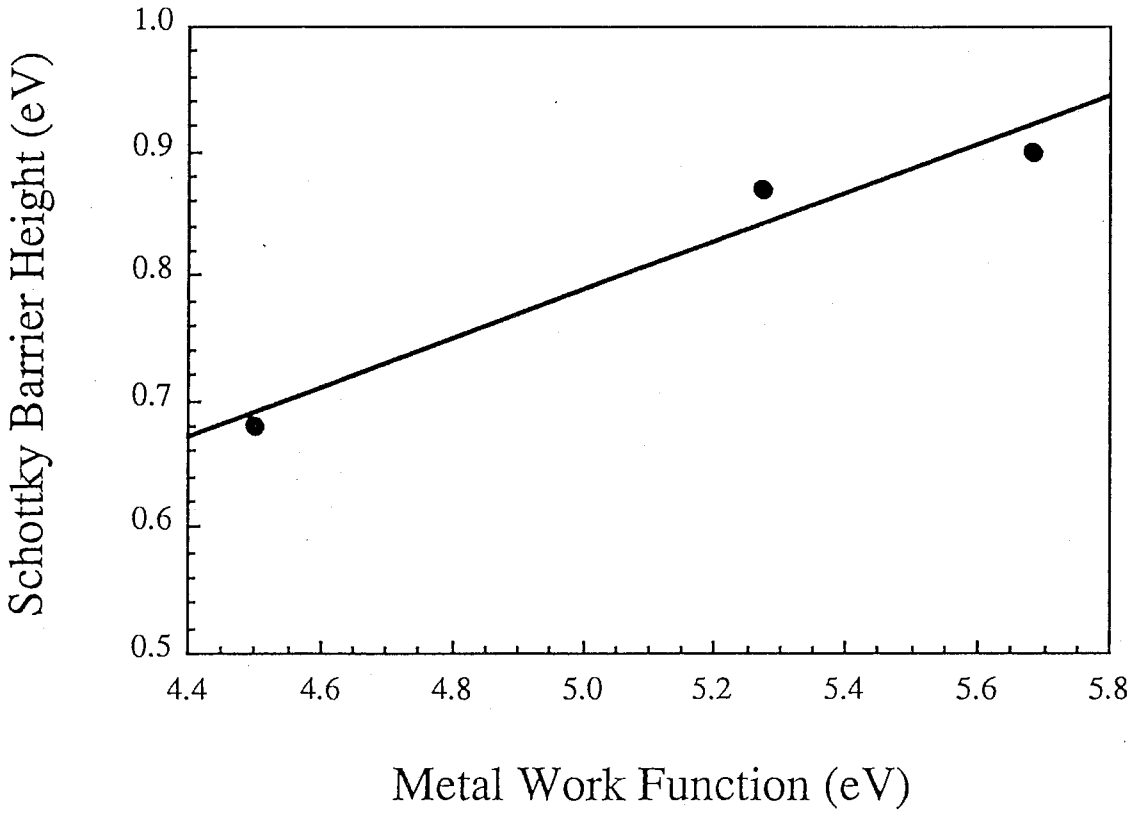

Schottky Barrier Height (eV)
1.0
0.9
0.8
0.7
0.6
0.5
4.4
4.6
4.8
5.0
5.2
5.4
5.6
5.8
Metal Work Function (eV)

Fig 7

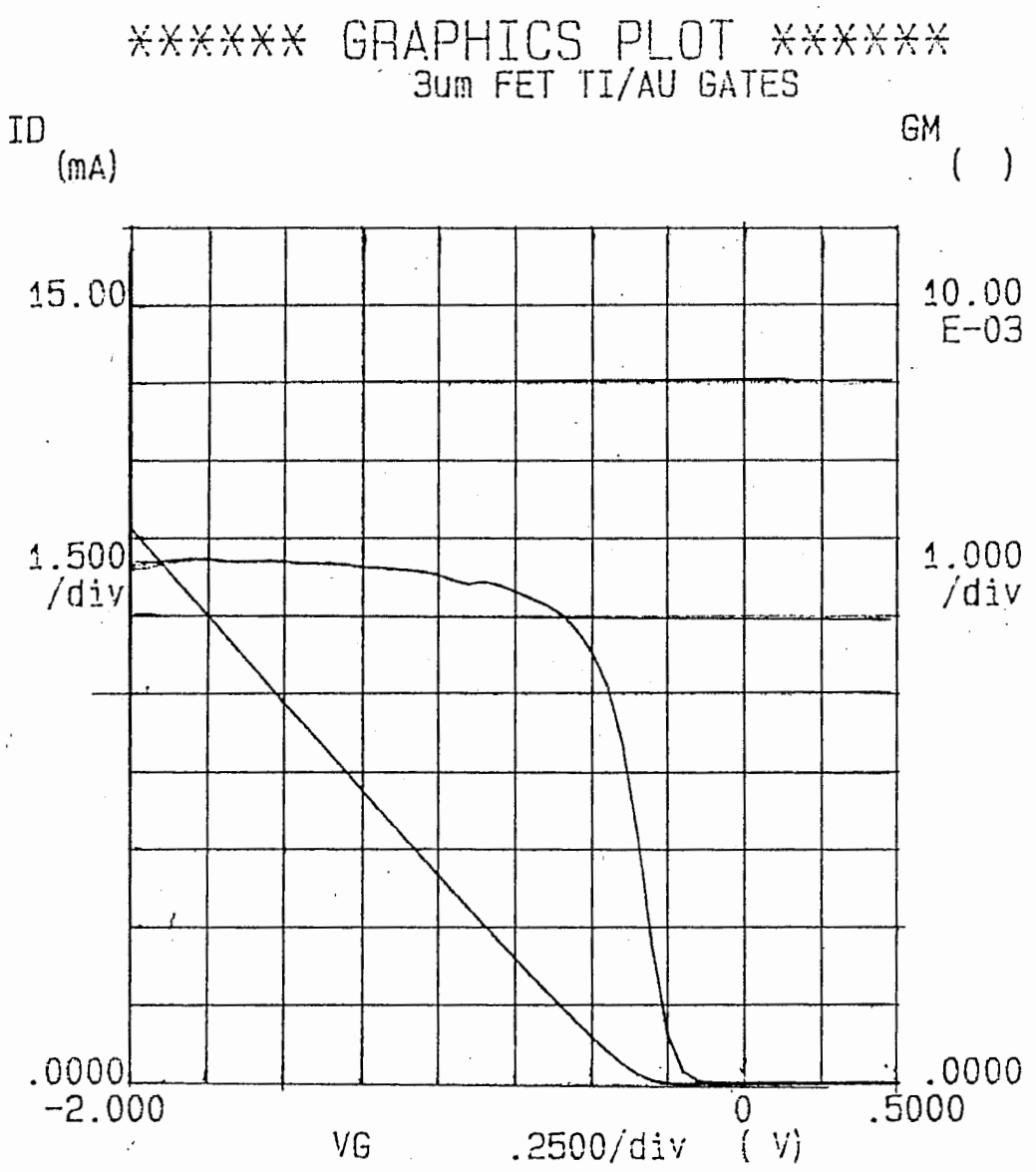

****** GRAPHICS PLOT ******
3um FET TI/AU GATES
ID
(mA)
GM
( )
15.00
1.500
/div
.0000
-2.000
10.00
E-03
1.000
/div
.0000
0
.5000
VG
.2500/div
(V)

Fig 8

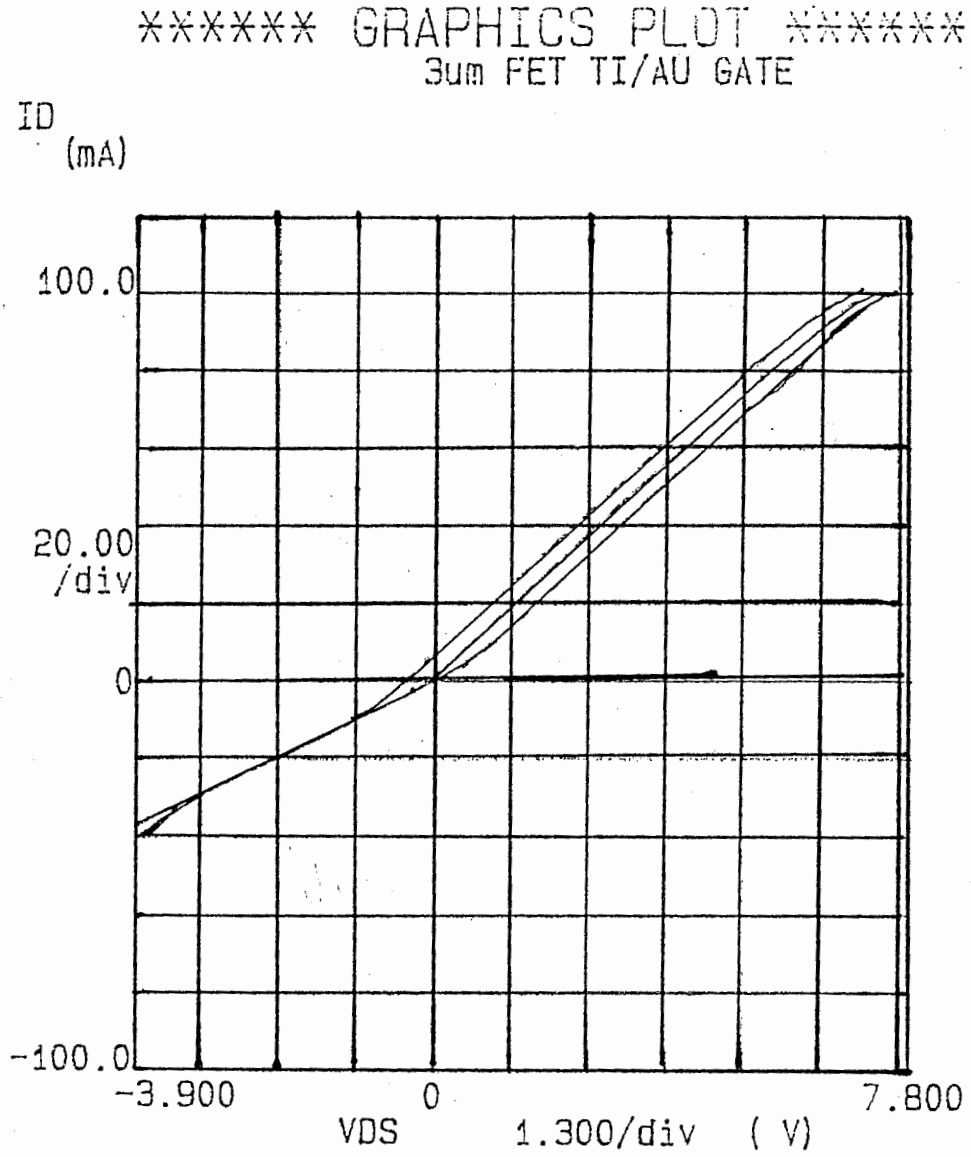

****** GRAPHICS PLOT ******
3um FET TI/AU GATE
ID
(mA)
100.0
20.00
/div
0
-100.0
-3.900
0
7.800
VDS
1.300/div
(V)

Fig 9

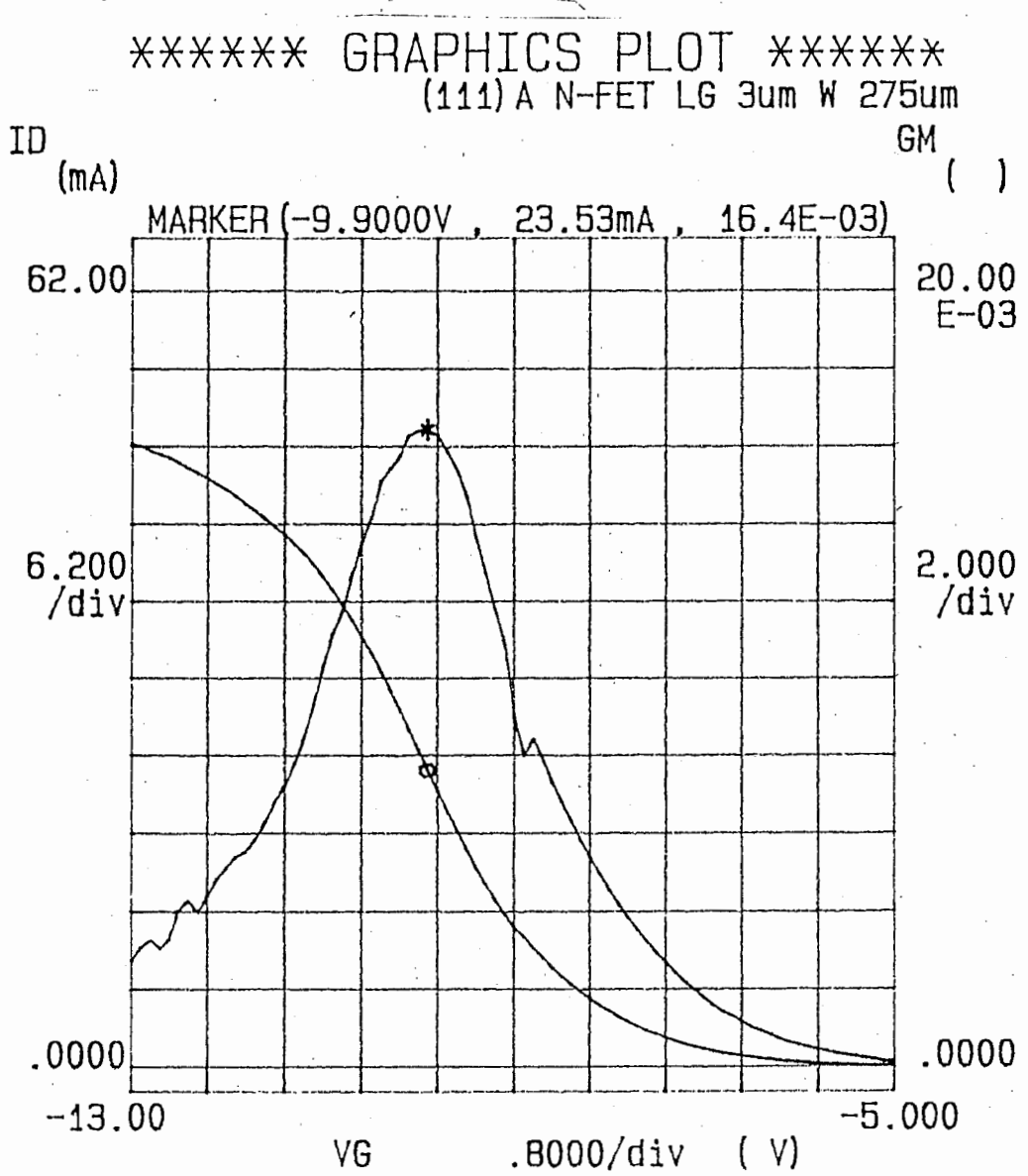

****** GRAPHICS PLOT ******
(111) A N-FET LG 3um W 275um
ID
(mA)
GM
( )
MARKER (-9.9000V , 23.53mA , 16.4E-03)
62.00
20.00
E-03
6.200
/div
2.000
/div
.0000
.0000
-13.00
-5.000
VG
.8000/div
(V)

Fig 10

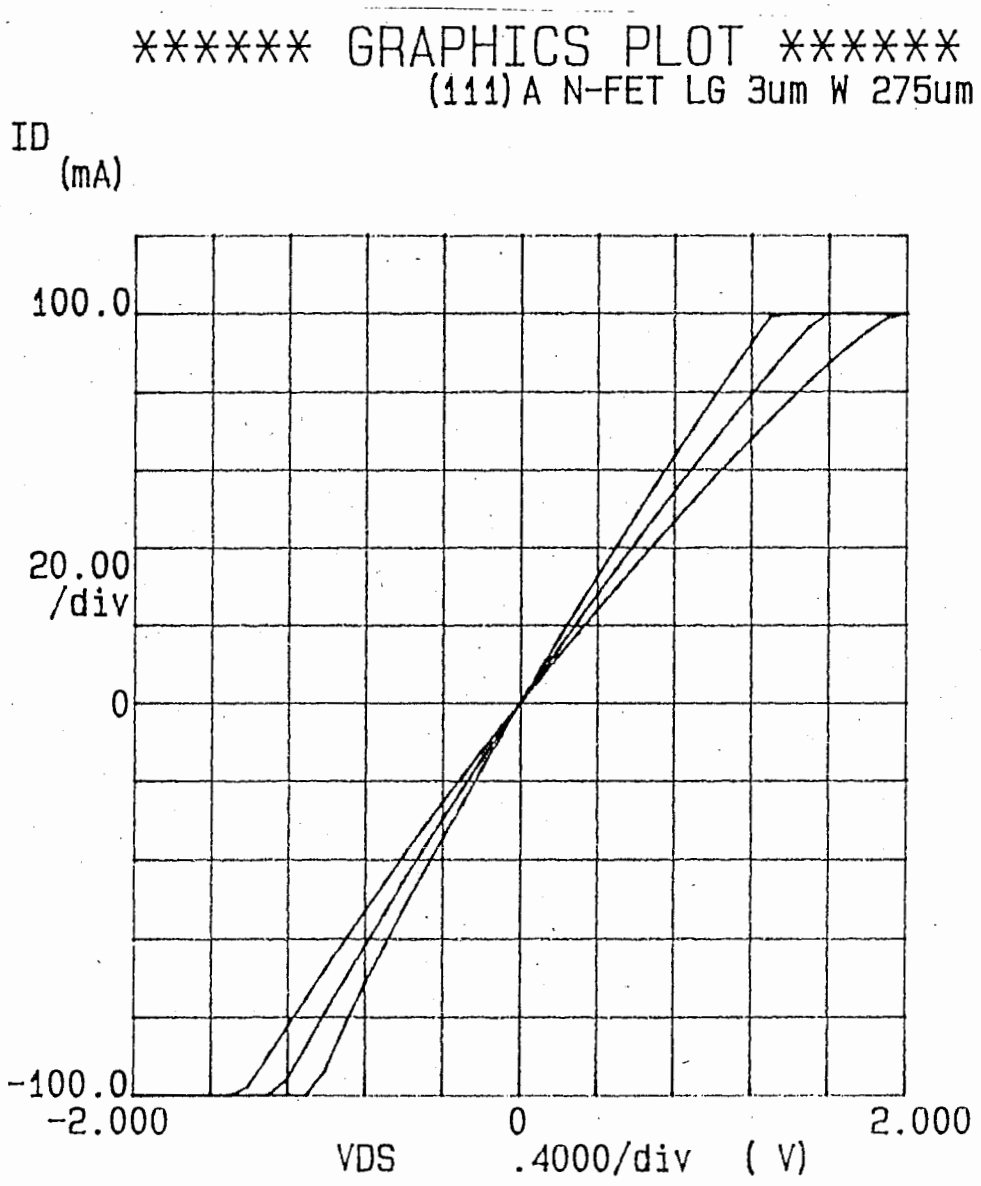

****** GRAPHICS PLOT ******
(111) A N-FET LG 3um W 275um
ID
(mA)
100.0
20.00
/div
0
-100.0
-2.000
0
2.000
VDS
.4000/div
(V)

Fig 11

ALLOY FURNACE TEMPERATURE DISTRIBUTION

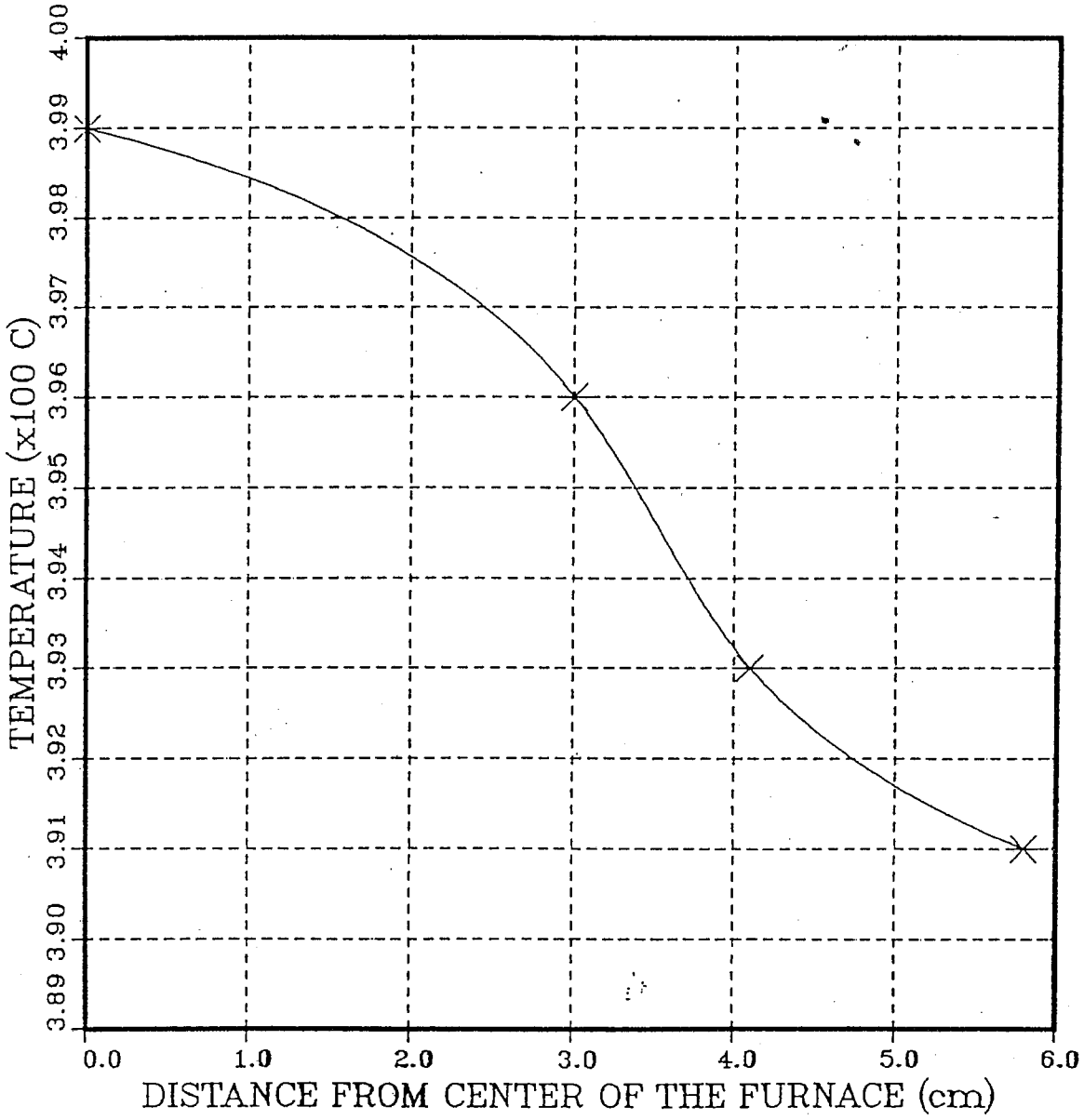


Fig 12