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ATRにおける高周波回路の研究
---超小型·高機能MMIC---

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概 要

報告者は昭和61年9月から平成2年1月までATRに在籍し、無線通信第二研究室のMMICグループリーダとして将来に向けた超小型·高機能な高周波回路の研究を推進した。室長は相川室長(昭和61年3月～平成1年1月)および赤池室長(平成1年2月～)である。本レポートは、報告者がモノリシックマイクロ波集積回路(MMIC)について提案した新しい構成·設計概念と、これを具体化した超小型·広帯域MMICをまとめたものである。まとめるに当たっては、ATR MMICの基本理念と特徴に重点を置き、今後の発展の一助となるよう心掛けた。

MMICグループは以下の研究員で構成された。

徳満主任研究員 (MMIC回路構成法の研究: S61.9～H2.1)
中本　研究員 (MMICプロセスデバイスの研究: S62.3～)
原　研究員 (MMIC回路設計法の研究: S61.9～H1.9)
平岡　研究員 (MMIC非線形デバイス回路の研究: S62.4～H2.2)
竹中研究技術員 (MMIC設計測定系の構成と回路特性評価の研究: S62.3～)
長谷川　研究員 (原研究員の後任: H1.10～)

尚、研究立上げにおいて、田中主幹研究員(S61.4～S63.1)の御協力を頂いた。

MMICの研究、特に世界に先駆けた新しい概念の創造とその具体化を効率良く行うためにはグループ全体の協力体制が重要であるため、全てのアイデアについて役割を適宜分担して研究を行った。報告者は、MMIC研究の技術的マイルストーンを当初に設定·図示するとともに、以下の新しい構成·設計概念を提案·具体化して上記のMMICグループを牽引した[1-17]。

① アクティブインダクタ
② 線路一体化FET: Line-Unified-FET (LUFET)
③ 多層薄膜構造: Multilayer MMIC
④ 基本回路機能モジュール組合せ

また、ハードウェアとしてのMMICを研究するには試作が不可欠であると判断し、試作メーカを当初に確保すると共に、直ちに回路設計を開始して試作を推進した。この第1次試作(昭和61年度)に引き続いて、第2次試作(昭和62年度)、第3次試作(昭和63年度)を行った[18-22]。試作メーカは主に三菱電機(株)である。第3次試作からは多層化MMICの研究を強化するため三洋電機(株)を追加した。

各研究員の成果については、原則的に、担当したMMICについて外部発表することとした。また、各研究員が少なくとも1回は海外のシンポジウムで発表することを目標とした。各研究員は回路シミュレーションおよび測定技術に習熟する過程において、報告者の推進するATR MMICの基本理念を体得し多くの成果を上げた[11-58]。

ATRにおける高周波回路の研究
-----超小型·高機能MMIC------

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1. はじめに
1. Introduction

ATR光電波通信研究所では、将来の無線通信用の超小型移動機や高機能アンテナの実現などを主な目的としてモノリシックマイクロ波集積回路(MMIC)の研究を行っている。更に、この研究を通して確立される技術が広くマイクロ波回路技術に影響を及ぼし、基盤技術になることを研究の目標としている。

未来の移動通信用無線送受信機をカードないし腕時計ほどに超小型化することは、この分野の研究者の夢の一つである。この場合、回路については現在のMMICの集積度を大幅に高める必要がある。また、サービスの向上および多様化も要望され、装置機能の大幅な向上が必要である。周波数帯もマイクロ波からミリ波までサービスに応じて使い分けることになると思われる。それを実現するための基盤技術の一つとして我々は、マイクロ波·ミリ波帯の送受信系と高速高機能な信号処理系を1ないし2チップに集積化することを技術的最終ターゲットとしてMMICの研究を取り上げた。

図1.1は腕時計型移動機の想定図および現状の移動機との容積比較を示す。我々の研究テーマは図中の「移動機回路」(共用部、無線部、制御部、配線、空間)の小型化·高機能化である。従来のハンドヘルド移動機の容積は約400cc(B型移動機 [1.1]; NTT)ないし約200cc(マイクロタック; MOTOROLA)である。最近容積150cc程度のハンドヘルド移動機の開発が進められている。しかし、従来のMMIC技術を100%適用して全IC化したとしても100cc以下の容積でハンドヘルド移動機を実現することは困難である[1.1]。これに対して、腕時計型移動機に想定される容積は僅か16ccである。移動機回路についてみると、全IC化の場合に対しても1/30以下の小型化(30倍以上の高集積化)が要求される。

図1.2は、ATRにおけるMMIC研究の技術的マイルストーンを示したもので、マイクロ波回路を半導体基板の片側に「積み重ねる」という発想を基にしている。各マイルストーンを、①共平面小型化MMIC、②多層化MMIC、③立体化MMICと名付ける。図の最上部に示す従来のMMICは半導体基板の裏側に接地導体を有し、表側平面にトランジスタおよび金属配線からなるマイクロ波受動回路等を形成している。しかし、受動回路の寸法は半導体基板厚および波長に依存するため小型化が困難であり、MMICチップ表面の殆どの部分が受動回路で占められる。このため、増幅器、ミクサといった単一機能回路(simple function block)でも5mm^{2}より小型に実現することは容易でなかった。最近の3ないし4年間の外部動向としては、FETを能動素子および電圧制御可能な受動素子として多数使用する能動化MMIC [1.1-1.7]、線路導体と接地導体が同一平面にある伝送線路とその特徴を用いるUni-Planar MMIC [1.8-1.10]、プッシュプル構成によって非常に小さく実現される増幅器を種々の用途に用いて組み合せるモジュール構成のMMIC [1.11-1.13] 等が提案され、2mm^{2}程度(最小で約1mm^2)の小型、広帯域MMICが多く報告されるようになった。これらのMMICは基本的に半導体基板の厚みに依存しない回路構成を指向している。しかし、ATRが目指す小型化·高集積化には程遠く、かつ、これ以上の小型化は望めない。我々のMMIC研究はこれらの問題を解決するものである。このために報告者は、「線路一体化」や「多層化」といった新しい回路構成概念を提案し、かつ、これらの具体化を行った。現在までに、共平面小型化MMICと多層化MMICの研究を並行して進めてきた。立体化MMICについては、プロセス技術の研究を東京工業大学の古川静二郎教授に委託している(平成元年度)。

共平面小型化MMICは「線路一体化FET」によって特徴付けられる。線路一体化FET(Line-Unified-FET: LUFET)は、FETの電極配置内に形成されるコプレナ線路やスロット線路(総称して、共平面

線路)間の電気的関係をエアブリッジ等により一義的に決定することによって得られる、FETに近い形状·寸法の回路機能モジュールである。つまり、「デバイス即ち機能モジュール」である。種々のLUFETを組み合せることによりMMICの大幅な小型化(1/3~1/10)が可能となる。これまでに、基本となる分配·合成LUFETを整理し体系化すると共に、これらの基本LUFETの変形および組合せにより、従来小型化·広帯域化が容易でなかった機能回路(マジックT, スイッチ: 合成·分配回路, ミクサ: 位相反転回路, 変調器: 逓倍器: サーキュレータ等)を僅か0.1mm^{2}ないし1mm^{2}の半導体表面に実現して上記の効果を明らかにした。ここで、LUFET MMICにおける重要な設計手順は上記の「変形」(modification)および「組合せ」(combination)である、ということが重要である。「変形」によってLUFETの形状内に種々あるいは複数の回路機能を閉じ込め、「組合せ」によって回路機能を集積する。研究成果の概要を図1.3および図1.4に示す。

多層化MMICは、共平面小型化MMIC上にマイクロ波受動回路を多層化したもので、さらに小型化·高集積化を可能にする。我々のいう多層化とは、半導体基板の片平面に形成される接地導体やストリップ状の導体の上部に厚さ数μmの誘電体絶縁膜(dielectric thin film)を数層積み重ね、その層間·層上に種々の形状·作用の導体を配置する概念を指す。これにより、マイクロ波線路および受動回路を立体的に構成することができる。またこの構成では、マイクロ波線路の基板厚は誘電体の膜厚に等しい(数μmないし10μm)ので、線路の形状寸法を非常に小さくすることができる。さらに、これらの構造的特長を活かして種々の新しいマイクロ波線路および超小型マイクロ波受動回路(従来の1/10以下)を実現することができる。これまでに、形状·寸法が非常に大きいため従来のMMICでは殆ど使用されなかった1/4波長線路の小型化を、多層化マイクロ波線路の一つとして新しく提案した「薄膜マイクロストリップ線路」(Thin Film

Microstrip (TFMS) Line)を用いて実現(0.2mm^{2}以下)した。更に、線路交差(line crossover)·縦方向配線(vertical connection)·異層配線(lines on two different layers)等の利点をも活かして、種々の受動回路(90度·180度ハイブリッド,マジックT,多端子分配回路,分布型増幅器等)を1mm^{2}以下の寸法で実現し、上記の効果および高集積化の可能性を明らかにした。図1.5に研究成果の概要を示す。

最終段階である立体化MMICは、上記の半導体/誘電体膜構造を複数積層する構造で、これにより、一層の高集積·高機能化を目指す。MMICの立体化のためには多層誘電体膜上に半導体(GaAs, Si)層を形成する技術の進展が必須条件である。

以下、第2章にて線路一体化FETおよびこれを変形あるいは組み合せて実現したLUFET MMICについて述べる。第3章では多層化MMICについて、誘電体膜形成プロセス、マイクロ波·ミリ波伝送線路、およびTFMS線路を用いた多層化MMICについて述べる。尚、各節毎に図をまとめ、基本的な考え方を理解しやすくするように努めた。また、参考文献は各章毎にまとめ、各章で述べる内容の背景が分かるようにした。

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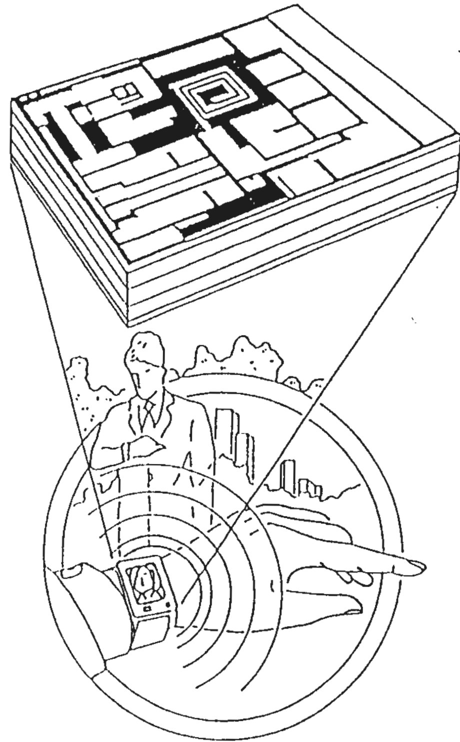
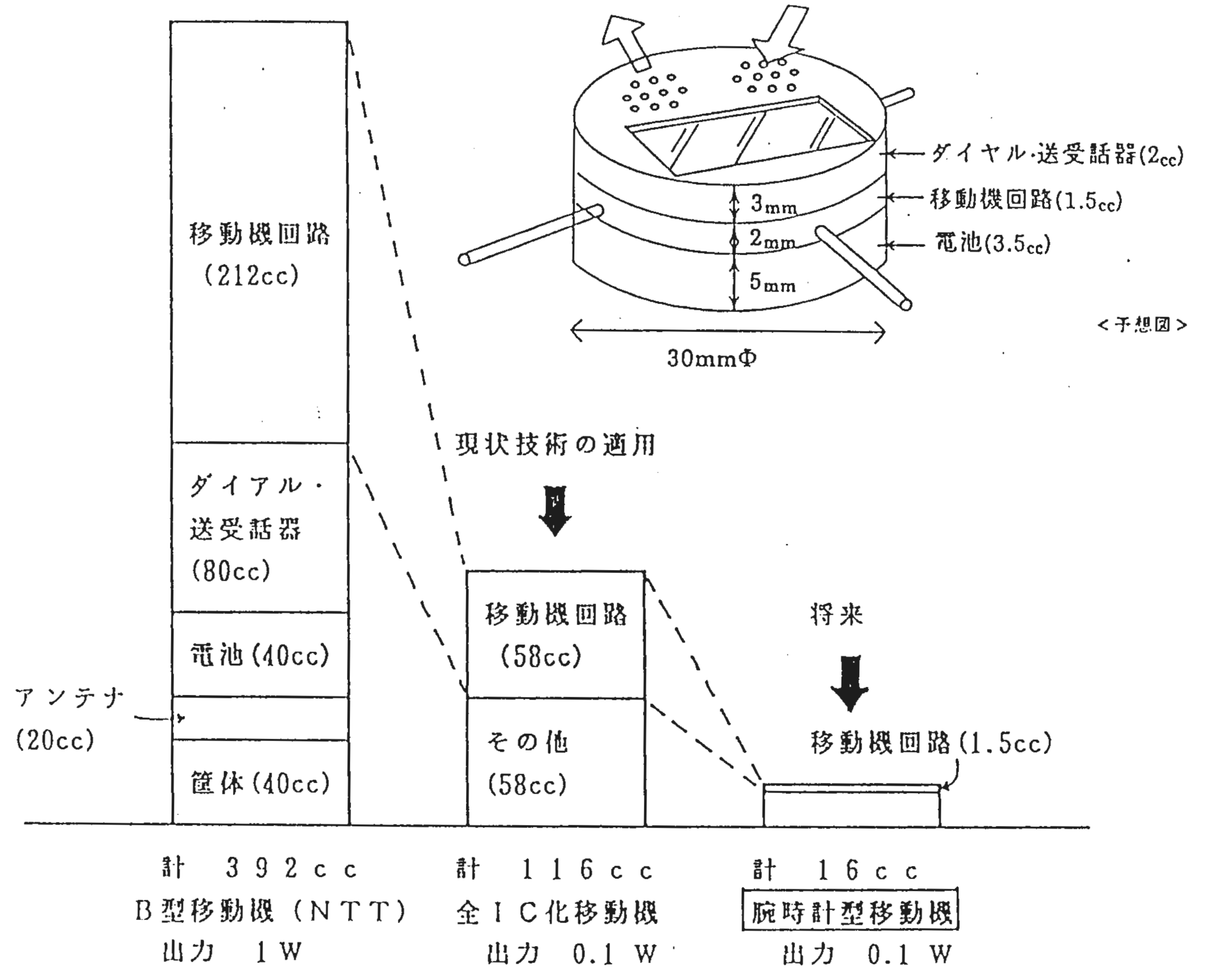
図1.1 超小型移動無線機とMMIC研究

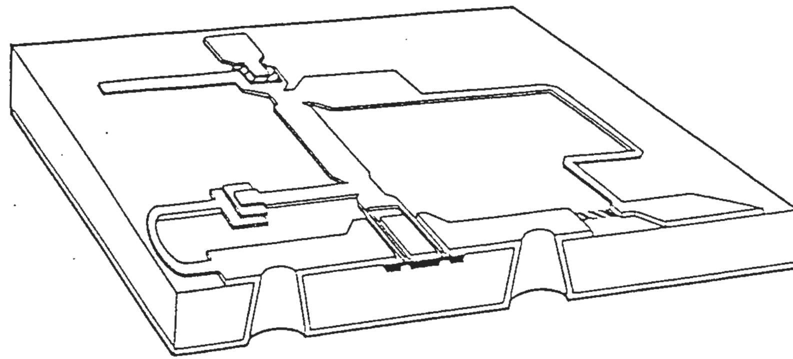
ATR





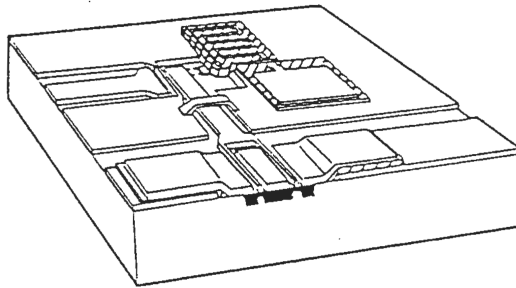
(注)移動機回路： 共用部、無線部、制御部、配線・空間

図1. 2 MMIC研究の技術的マイルストーン



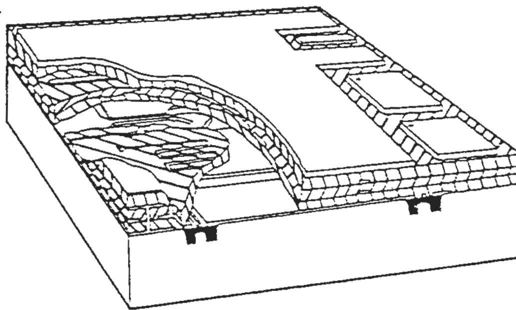
現状のMMIC

集積度: 1倍



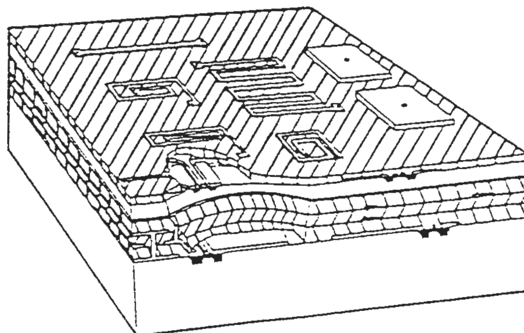
共平面小型化MMIC

集積度:~3倍



多層化MMIC

集積度:~10倍

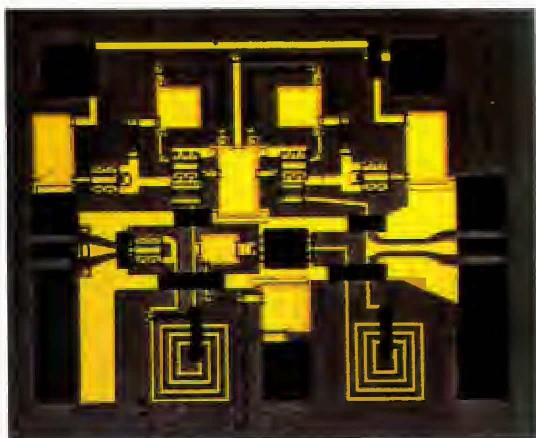


立体化MMIC

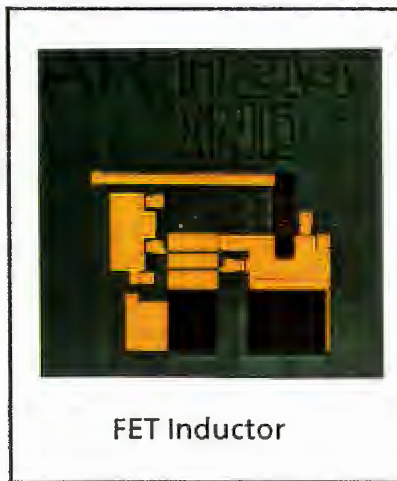
集積度:~30倍

図1. 3 共平面小型化MMIC

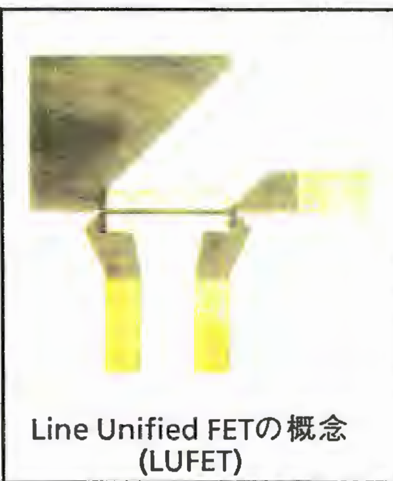
マイクロ波回路能動化·小型化の発想



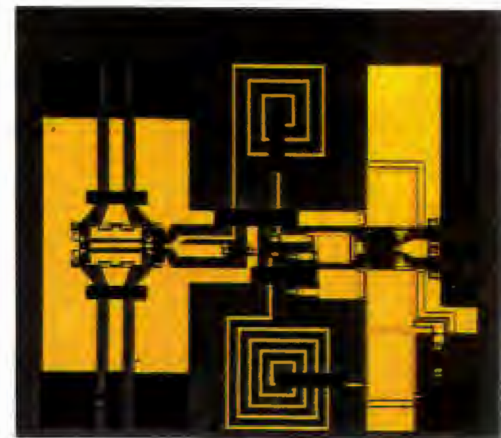
広帯域増幅器
(0.1-10GHz)
1.0mm×1.3mm



FET Inductor

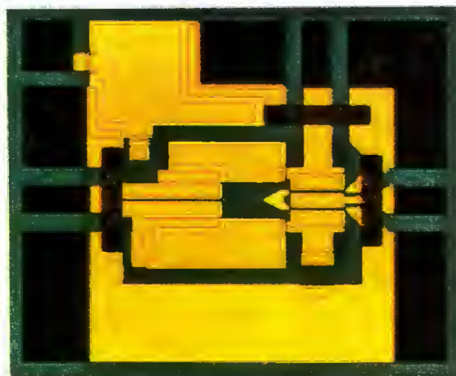


Line Unified FETの概念
(LUFET)

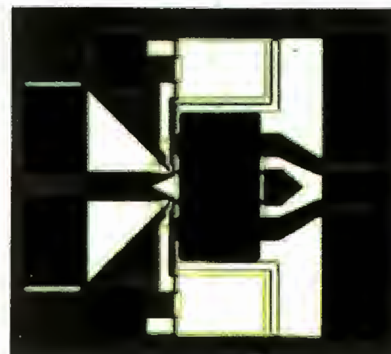


電力合成器、ミクサ
(1-12GHz)
0.9mm×1.4mm

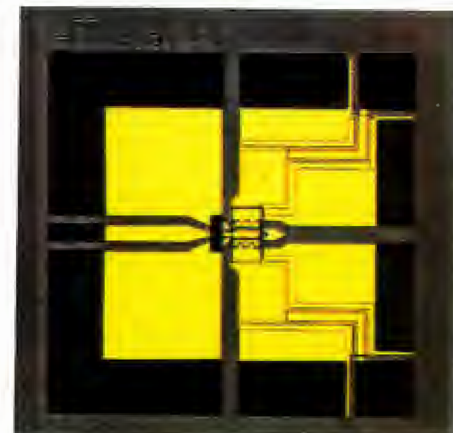
逓倍器
(3-10GHz)
0.5mm×0.5mm



アイソレータ
(1-15GHz)
0.5mm×0.6mm

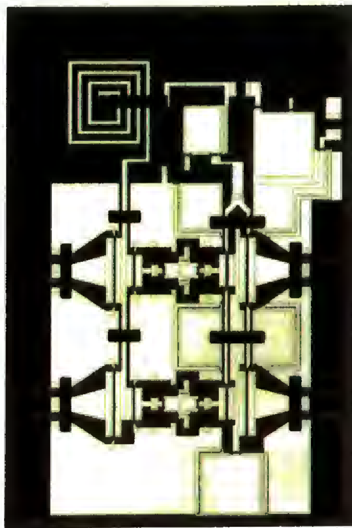


平衡変調器
(1-18GHz)
0.5mm×0.6mm



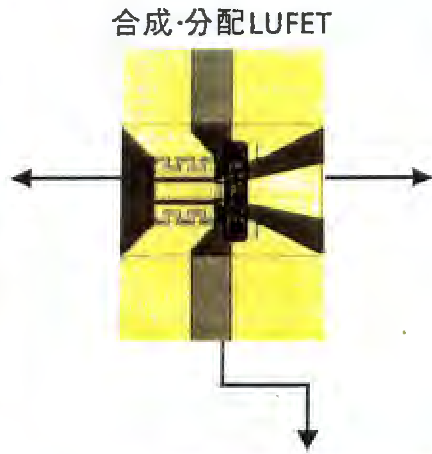
マジックT
(1-18GHz)
1mm×1mm

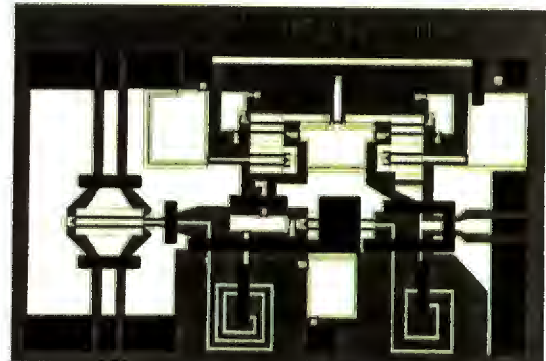
図1.4 LUFETを用いたモジュール化設計



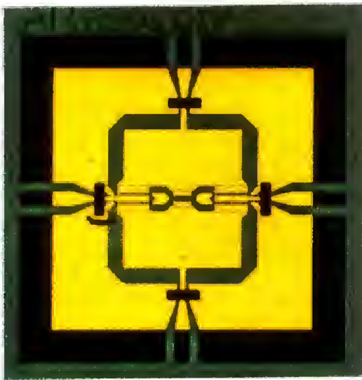
多端子合成/分配器

合成·分配LUFET

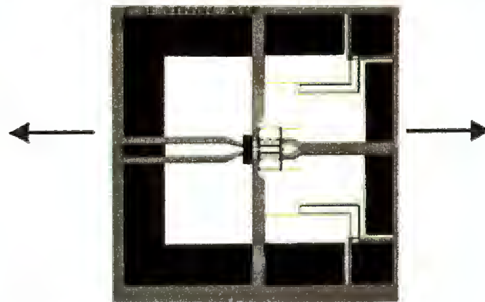




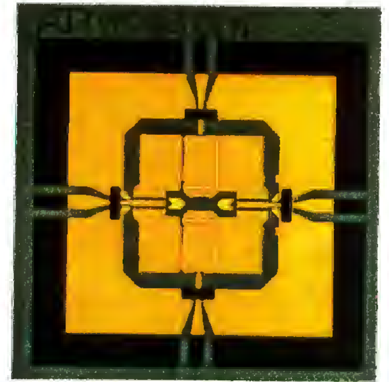
無損失合成器、ダウンコンバータ、アップコンバータ



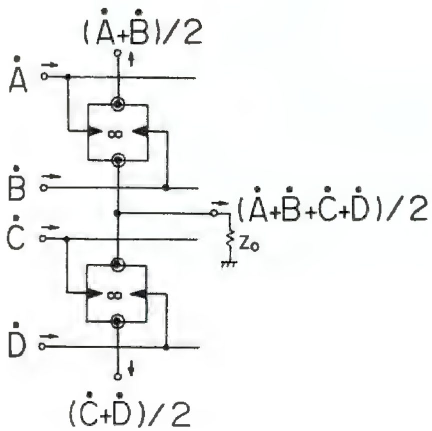
信号合成·信号経路切替え器



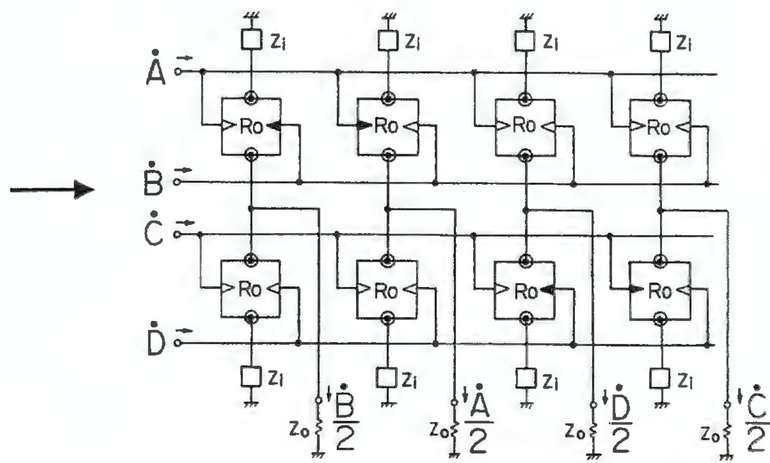
マジックT LUFET



方向性信号分配器



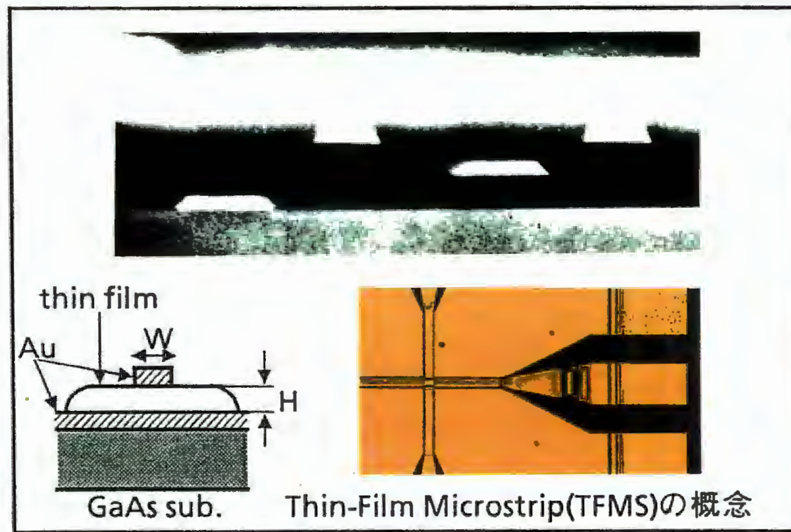
多端子合成器



4×4スイッチマトリックス

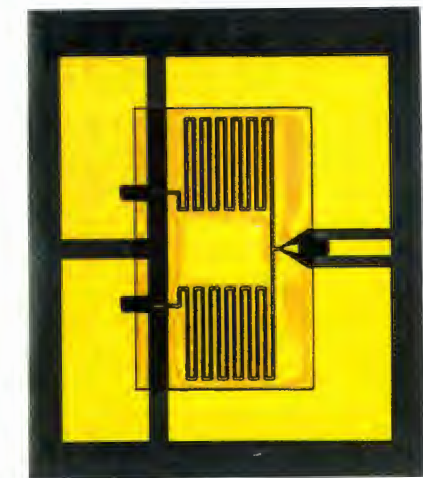
図1. 5　多層化MMIC

マイクロ波回路積重ねの発想

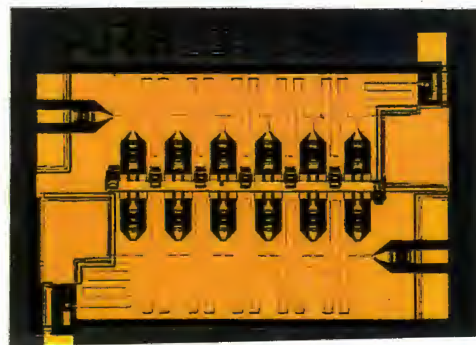


Thin-Film Microstrip(TFMS)の概念

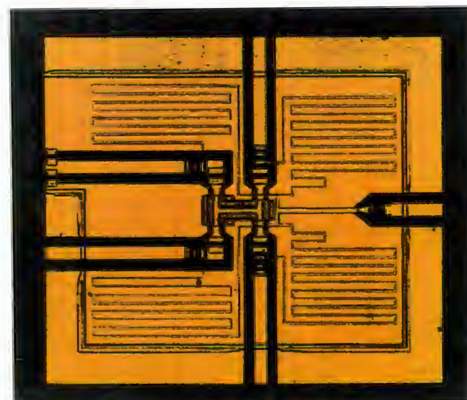
マジックT
(4-18GHz)
0.9mm × 1.0mm



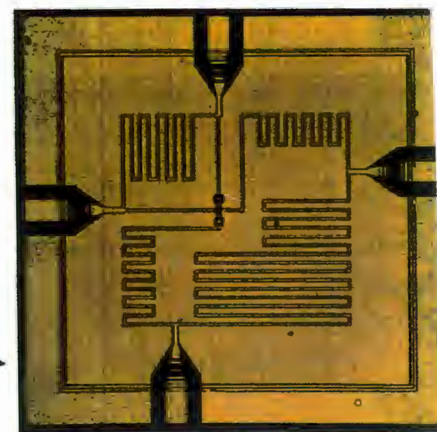
マジックT
(4-18GHz)
0.9mm × 1.0mm



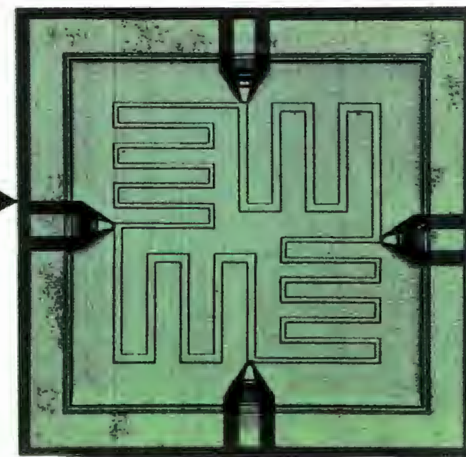
分布型増幅器
(1-12GHz)
0.8mm × 1.3mm



4端子ウィルキンソン電力分配器
(10-15GHz)
0.9mm × 1.0mm



端子入替え型
ラットレース・
ハイブリッド回路
(17-23GHz)
1.3mm × 1.3mm



ブランチライン・ハイブリッド回路
(10-14GHz)
1.3mm × 1.3mm

2. 線路一体化FET(LUFET)MMIC
2. Line-Unified-FET(LUFET)MMIC

In a sense, MMIC technology has been recently matured. MMIC application to various microwave and millimeter-wave components has become more practical, although the chip size is still not small enough to realize one-chip multifunction MMICs composed of signal processing functions. Combiners and dividers, in phase and out of phase, are fundamental and important parts of MMICs at various levels of integration. In recently reported MMICs, active devices are often combined with microstrip T junctions, instead of quarter-wavelength transmission lines. This allows compact microwave combiners and dividers [2.1-2.3], where the distributed amplifier architecture is of practical use in MMIC combiners and dividers due to compact size and ultra-wide-band characteristics. However, the circuit configuration is still large and extremely complicated because several GaAs FETs and many inductive lines or spiral inductors are packed on a chip. It is not the best way to widely implement such combiners and dividers on a multifunction MMIC chip, when small chip size and a higher level of integration is required.

The purpose of our work is to realize miniaturized and broadband function blocks with very simple configurations for multifunction monolithic microwave circuits. The "Line-Unified-FET" (LUFET), which is proposed and developed in ATR, mitigates the size and complexity problem considerably, and expands the application of combiner and divider to various multifunction MMICs. In section 2.1, the LUFET MMIC and conventional MMIC are compared in size. Basic combiner and divider LUFETs, in phase and out of phase, and some effective modifications which offer functionally enhanced LUFETs are proposed and demonstrated in section 2.2. The "modification" of basic combiner and divider LUFETs allows integrating various circuit-function in a very small area. Magic T LUFET which is one of the typical modified LUFET is described in detail in

section 2.3. The following section 2.4 demonstrates applications of the LUFETs to RF signal processing elements such as multiport combiner/dividers, mixers, balanced modulators, signal path switches and circulators.

2.1. LUFETによる小型化の効果
2.1. Chip Size Comparison

Fig. 2.1 compares the area of MMIC composed of the LUFETs (LUFET MMIC) and conventional, simple function MMIC. Dots and crosses representing conventional MMICs and circles representing LUFET MMICs are shown at the highest operating frequency of each MMIC. Larger circles represent the area of basic combiner and divider LUFETs. The dots and crosses show actual chip areas of broadband and narrow band MMICs, respectively, reported in four years of Monolithic Integrated Circuit Symposium Digests [2.4]. MMICs employing the distributed-line-based design approach occupy areas along or above the $(\lambda g/4)^2$ curve [2.5], and those using lumped circuit elements and a distributed amplifier configuration exhibit a relatively constant area of between 2 and 5mm^2. Frequency converter MMICs based on an extensive use of miniaturized push-pull amplifiers, which are produced by Pacific Monolithics, record the minimum chip area, approximately 1mm^2, while the area increases up to 2mm^2 or more as the frequency approaches the Ku-band [2.6-2.8]. On the other hand, the area of the fabricated LUFETs and LUFET MMICs which will be described below is less than 1.5mm^2; around 0.5mm^2, and that of the smallest one approaches 0.1mm^2 because the basic circuit functions are packed in a very small area nearly equal to that of a conventional FET.

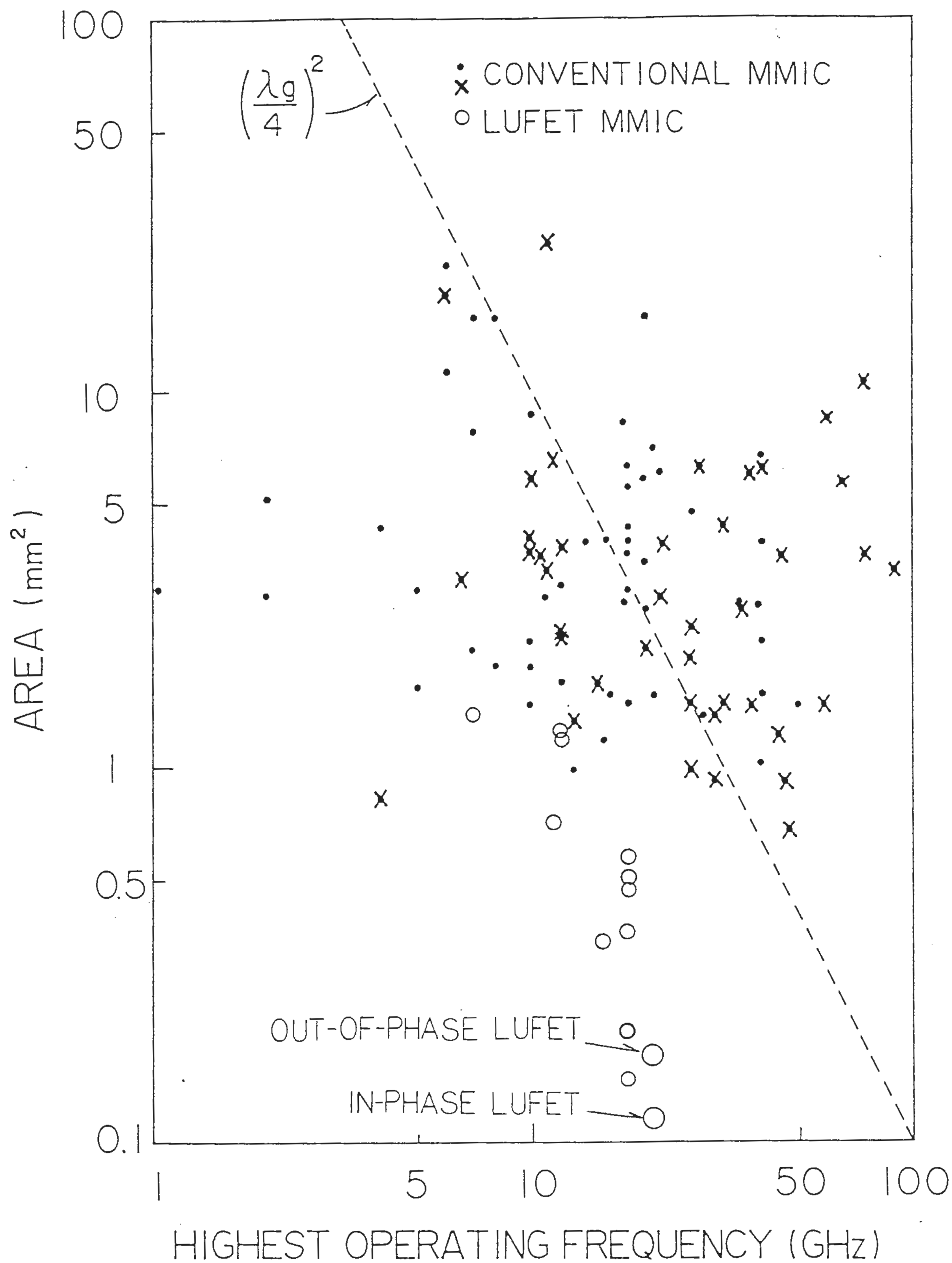


Fig. 2.1 Chip-size comparison of LUFET MMIC and conventional MMIC. Circles representing LUFET MMIC, and dots and crosses representing conventional, broadband and narow band MMICs are shown at the highest operating frequency of each MMIC.

2.2. 基本LUFETとその変形
2.2. Basic Com. and Div. LUFETs and Modifications

FET-sized combiner and dividers, in phase and out of phase, based on novel Line-Unified-FET (LUFET) concept, and some effective modifications such as extended combiner LUFETs, magic T LUFETs and phase inverter LUFETs are proposed and demonstrated. The "modification" of basic combiner and divider LUFETs allows to realize various circuit-function in a very small area. The area of fabricated LUFETs is between $0.1mm^2$ and $0.3mm^2$, and the operating frequency bandwidth approaches 20GHz.

The LUFET is constructed simply by establishing the relationships among the coplanar lines, which are formed within FET-electrode locations, for example, by using airbridge connecting electrode strips for the common electrode. The LUFET has the following features:

(a) the FET electrodes are unified coplanar waveguides or slotlines, and an FET as a three-port microwave "device" can serve as an active microwave "circuit-function module";

(b) ultra-wide-band operation due to the absence of frequency dependent distributed lines can be achieved;

(c) the coplanar waveguides and slotlines can be actively impedance matched with FETs below the FET cutoff frequency f_T, when the FET gates or drains are used for the common electrode.

2.2.1. 同相分配·合成LUFET
2.2.1. In-Phase LUFETs

Typical in-phase combiner LUFETs and divider LUFETs are illustrated in Fig. 2.2. The arrow in Fig. 2.2 shows the schematic expression of the electric field in the slotline and CPW. These LUFETs have FET electrode locations of source(S)-gate(G)-drain(D)-gate(G)-source(S) or D-G-S-G-D, and a pair of the

same electrode strips connexted through an airbridge are used for the common electrode. This is because the output port ③ of the combiner LUFETs and the input port ① of the divider LUFETs should be CPW for in-phase operation.

Fig. 2.2 (a) shows the configuration of a common-gate combiner LUFET, where the gate electrode strips are connected through an airbridge on one side [2-9]. When the gates are the common electrode of the module, a CPW is formed in the G-D-G structure. There are two slotlines in S-G structures. The slotlines and the CPW are related to one another through unilateral FETs as shown in the equivalent circuit diagram, and unified in the electorde locations. Therefore, when the slotlines and the CPW are used for input ports ①, ② and output port ③, respectively, the LUFET functions as an in-phase combiner module with low input impedances and a high output impedance. The input impedances are approximately equal to the reciprocal of each FET transconductance g_m corresponding to each S-G-D structure, up to frequencies approaching the FET cutoff frequency f_T. Fig. 2.2 (c) shows the configuration of a common-source combiner LUFET which has the same electrode locations as the common-gate combiner LUFET, Fig. 2.2 (a), and an amplification function. The source strips acting as the common electrode are connected through an air-bridge resulting in an output CPW (S-D-S) and two input slotlines (G-S). Fig. 2.2 (b) shows the configuration of a common-drain combiner LUFET. Fig, 2.2 (b) and Fig. 2.2 (c) are obtained in a similar fashion because the only change is in the FET electrode locations: from S-G-D-G-S to D-G-S-G-D, by means of a bias voltage change. This LUFET has high input impedances and a low output impedance reciprocally equal to the sum of the FET transconductances ($2g_m$). All of these LUFETs exhibit ultra-wide-band isolation characteristics from the output port to each input port and between the two input ports because of the unilateral characteristics of FETs. Furthermore, the constantly low impedance characteristics mentioned above provide an active impedance matching which eliminates additional matching circuitry.

In-phase divider LUFETs shown in Fig. 2.2 (d), (e), and (f) have functions similar to the in-phase combiner LUFETs except that they divide, rather than combine, signals. Fig. 2.2 (d) is the common-gate type, Fig. 2.2 (e) the common-drain type, and Fig. 2.2 (f) the common-source type. Table I summarizes coupling gains of the in-phase combiner and divider LUFETs (a)-(f), where FETs are assumed to be a combination of the transconductance and negligibly small gate-source capacitance only. The low impedance ports are impedance matched due to the condition in the parenthesis. Z_1 and Z_2 are input- and output port impedances respectively. The S parameters of LUFETs (a) and (e) measured in an on-wafer, 50Ω system are shown in Figures 2.3 and 2.4 to varify the wideband characteristics. In Figures 2.4 and 2.5 , the upper figure shows coupling gain and port isolation, and the lower one shows return loss. The characteristics are as follows up to 18GHz: insertion loss is less than 3dB; flatness of the insertion loss vs. frequency characteristic is less than 4dB peak-to-peak; return loss at the constantly low impedance ports is better than 15dB; port isolation is better than 15dB for the common gate type and better than 10dB for the common drain type.

2.2.2. 逆相分配·合成LUFET
2.2.2. Out-of-Phase LUFETs

Typical out-of-phase combiner LUFETs and divider LUFETs are illustrated in Fig. 2.5. These LUFETs have electrode locations of S-G-D-gap-D-G-S and D-G-S-gap-S-G-D for the common electrode configurations, and S-G-D-G-S and D-G-S-G-D for the other configurations, where "gap" means a spacing with a semi-insulating GaAs surface between the FET electorde strips such as drains and sources. No airbridge is used there because output port ③ of the combiner LUFETs and input port ① of the divider LUFETs should be excited in a balanced mode for out-of-phase operation. Therefore, these ports are slotlines. The

relationships among the unified coplanar lines are established by means of a symmetrical common electrode configuration.

Fig. 2.5 (a) shows the configuration of a common-gate combiner LUFET, where the gate electrode strips are connected with a metal plate on one side. When the gates are the common electrode of the module, a slotline T junction is formed between the plate (gate) and two drain strips. There are two slotlines in the S-G structures. The slotlines and the slotline series T junction are related to one another through unilateral FETs as shown in the equivalent circuit diagram. Therefore, when the slotlines and the T junction are used for the input ports and output port respectively, the LUFET functions as an out-of-phase combiner module with low input impedances ($1/g_m$) and a high output impedance. Fig. 2.5 (b) shows the configuration of a common-drain combiner LUFET. When the drain electrode strip in the center of FET electrode locations is used for the common electrode of the module, a slotline T junction is formed with the drain electrode strip and two source electrodes, one on each side of the strip. There are two slotlines in the G-D structures. The slotlines and the T junction are related to one another as shown in the equivelent circuit diagram. Therefore, when the slotlines and the T junction are used for the input ports and output port respectively, the LUFET functions as an out-of-phase combiner module with high input impeadanes and a low output impedance, that is, $2/g_m$ due to the output, slotline series T junction. Fig. 2.5 (c) shows the configuration of a common-source combiner LUFET. Fig. 2.5 (c) and Fig. 2.5 (b) are obtained in similar fashion because the only change is in the FET electrode locations: from S-G-D-G-S to D-G-S-G-D, by means of a bias voltage change. The LUFET has an amplification function and high input and output impedances. All of these LUFETs also exhibit ultra-wide-band isolation characteristics between input and output ports, and the constantly low impedances provide an active matching.

Out-of-phase divider LUFETs shown in Fig. 2.5 (d), (e), and (f) have configurations and functions similar to the out-of-phase combiner LUFETs except

that they divide, rather than combine, signals. Fig. 2.5 (d) is the common-gate type, Fig. 2.5 (e) the common-drain type, and Fig. 2.5 (f) the common-source type. Table II, like Table I, summarizes the coupling gains of the out-of-phase combiner and divider LUFETs (a)-(f). The S parameters of LUFETs (a) and (e) measured in a 50Ω system are shown in Figures 2.6 and 2.7 to varify the wideband characteristics. The widwband characteristics between 1GHz and 18GHz are almost the same as those of the in-phase LUFETs. The out-of-phase combining and dividing are achieved by the slotline series T junction in the whole frequency range.

2.2.3. 基本LUFETの変形

2.2.3. LUFET Modifications

The basic combiner and divider LUFET configurations in the previous sections are modified to realize functionally enhanced LUFETs. Some typical modifications are shown below.

A. Extended Combiner LUFET

Fig. 2.8 (a) shows an in-phase combiner LUFET with CPW input ports. This is realized simply by adding a ground on the other side of the LUFET shown in Fig. 2.2 (a) from the existing common electrode and, if needed, connecting all the grounds through airbridges. The modified and original LUFETs provide the same performance. Other LUFETs can be modified in a similar fashio. Fig. 2.8 (b) shows another extended combiner LUFET which is easily derived from the above modified LUFET. This LUFET has two CPW ports isolated from each other and two signal-through output ports. The characteristics of the LUFETs in Fig. 2.8 are easily estimated from those of the basic LUFET in Fig. 2.2 (a).

B. Magic T LUFET (will be described in detail in section 2.3)

Fig. 2.9 shows a 1-18GHz magic T LUFET [2.10-2.11] derived from the in-phase divider LUFET shown in Fig. 2.2 (d). A slotline T junction is formed with an additional conductive pad connecting the two gate electrodes and two drain electrodes, one on each side of the pad. As a result, two different dividers, in-phase and out-of-phase, are unified in the electrode locations. This magic T can be by itself, a magic T function block which is impedance matched at every port. The fabricated chip size is 1mm×1mm, while the intrinsic area after subtracting input- and output line areas is only 0.3mm×0.4mm. The measured performance between 1GHz and 18GHz is as follows: coupling loss from port Ⓗ or Ⓔ to ports ① and ② is within 5dB±0.5dB; return loss at each port is greater than 10dB;

isolation is greater than 20dB except between ports ① and ②, where it is 10dB. Various magic T LUFETs are derived from the other in-phase, combiner and divider LUFETs by using the separated electrodes as an additional slotline.

C. Phase Inverter LUFET

Fig. 2.10 shows a phase inverter LUFET derived from the out-of-phase, common source divider LUFET shown in Fig. 2.5 (e). The electrode locations S-G-D(C)-G-S are modified to C-gap-[S-G-D(C)-G-S]-gap-C by adding other electrodestrips for the common electrode (C) one on each side of the original LUFET, connecting these three common electrodes through airbridges, and coupling a pair of output slotlines ② and ③ to provide a CPW output port ④ for in-phase combining. One gate is in the on state and the other gate is in the off state when this LUFET serves as a phase inverter. No output is obtained when both gates are in the on state, because out-of-phase output signals with the same amplitude are combined in phase at port ④. The chip size is 0.6mm×0.5mm. Fig. 2.11 shows the measured performance of the phase inverter LUFET. Between 2GHz and 17GHz, insertion loss is 2dB, isolation is greater than 15dB, and output return loss is better than 10dB. A 180° phase shift is accomplished by the input slotline T junction. Other phase inverter LUFETs are realized by the in-phase combining of the output ports of out-of-phase divider LUFETs or the input ports of out-of-phase combiner LUFETs,

D. LUFETs Surrounded by a Ground

It is sometimes required to surround LUFETs by a ground for effective modular designs. Fig. 2.12 shows a method to surround the magic T LUFET with a ground. The slotlines fed to ports ①, ② and Ⓔ through thin film microstrip (TFMS) lines on a 9μm thick dielectric (SiON) film [2.12,13] (see chapter 3), are formed around the FET electrode locations, constituting an additional slotline T junction on the side of the LUFET opposite the CPW input port Ⓗ. The even- and

odd mode equivalent circuits for the magic T are represented, below 12 GHz, by those for the original magic T LUFET above, because the length of each slotline section is designed to be negligibly small compared to the operating frequency wavelength. This method is applicable to surround other LUFETs by a ground. The measured performance of the magic T surrounded by a ground is shown in Fig. 2.13: coupling loss from port Ⓗ or Ⓔ to ports ① and ② is within 5dB±1.5dB; return loss at each port is better than 10dB; isolation is greater than 20dB except between ports ① and ②, where it is about 10dB. The modified magic T shown in Fig. 2.12 results in a very small performance loss at frequencies below 12GHz. The chip size of this magic T is 1mm×1mm, and the intrinsic area covered by the dielectric film is $0.45mm^2$.

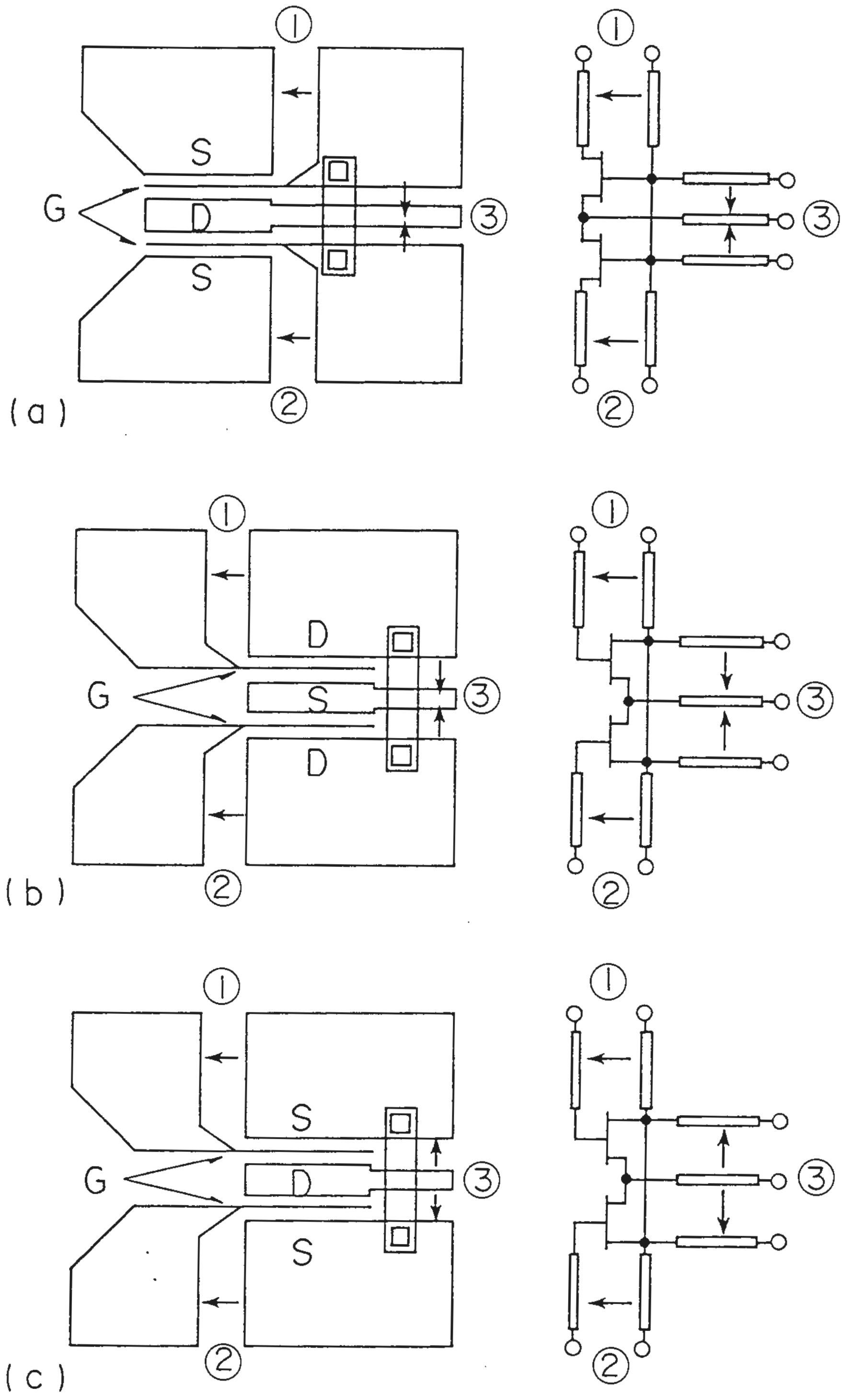


Fig. 2.2 Typical in-phase combiner and divider LUFETs and the equivalent circuit diagrams. (a)-(c) are combiner LUFETs and (d)-(f) divider LUFETs, where indicates an airbridge.

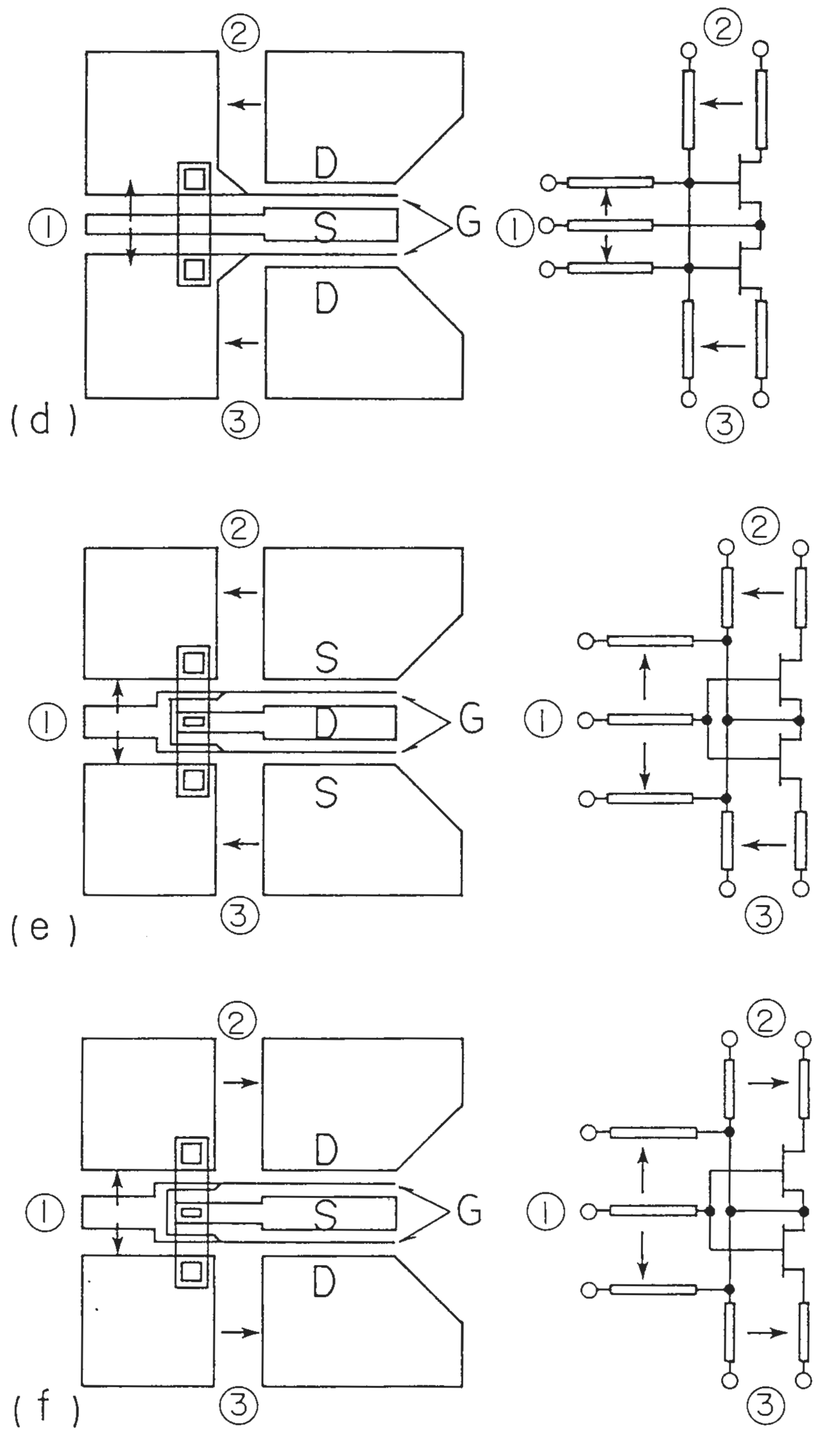


Fig. 2.2 Typical in-phase combiner and divider LUFETs and the equivalent circuit diagrams. (a)-(c) are combiner LUFETs and (d)-(f) divider LUFETs, where indicates an airbridge.

Table I
Coupling gain of in-phase combiner and divider LUFETs

type \ function	in-phase combiner	in-phase divider
common gate	(a) $\frac{2g_m\sqrt{Z_1Z_2}}{1+g_mZ_1}$ $(g_mZ_1=1)$	(d) $\frac{2g_m\sqrt{Z_1Z_2}}{1+2g_mZ_1}$ $(2g_mZ_1=1)$
common drain	(b) $\frac{2g_m\sqrt{Z_1Z_2}}{1+2g_mZ_2}$ $(2g_mZ_2=1)$	(e) $\frac{2g_m\sqrt{Z_1Z_2}}{1+g_mZ_2}$ $(g_mZ_2=1)$
common source	(c) $2g_m\sqrt{Z_1Z_2}$	(f) $2g_m\sqrt{Z_1Z_2}$

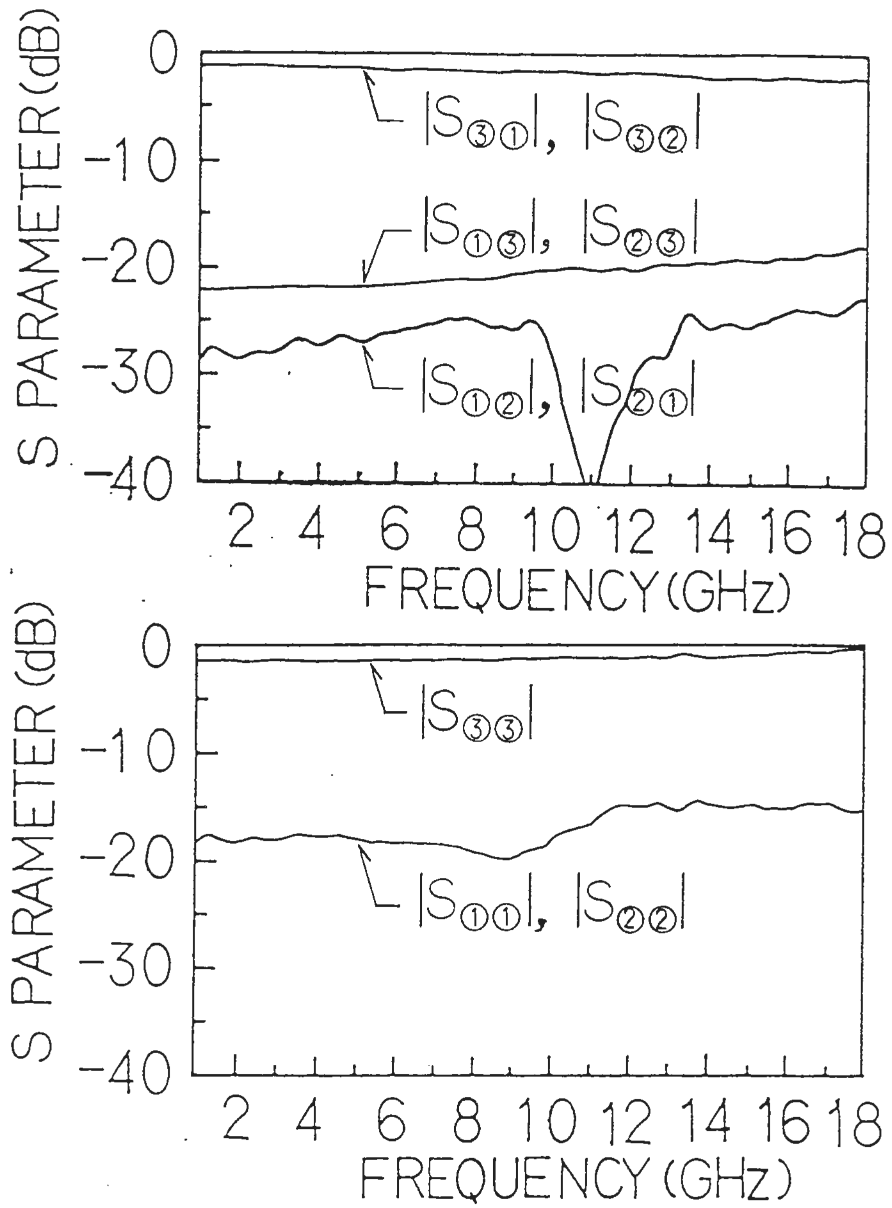


Fig. 2.3 S-parameters of the in-phase combiner LUFET (a) measured between 1GHz and 18GHz.

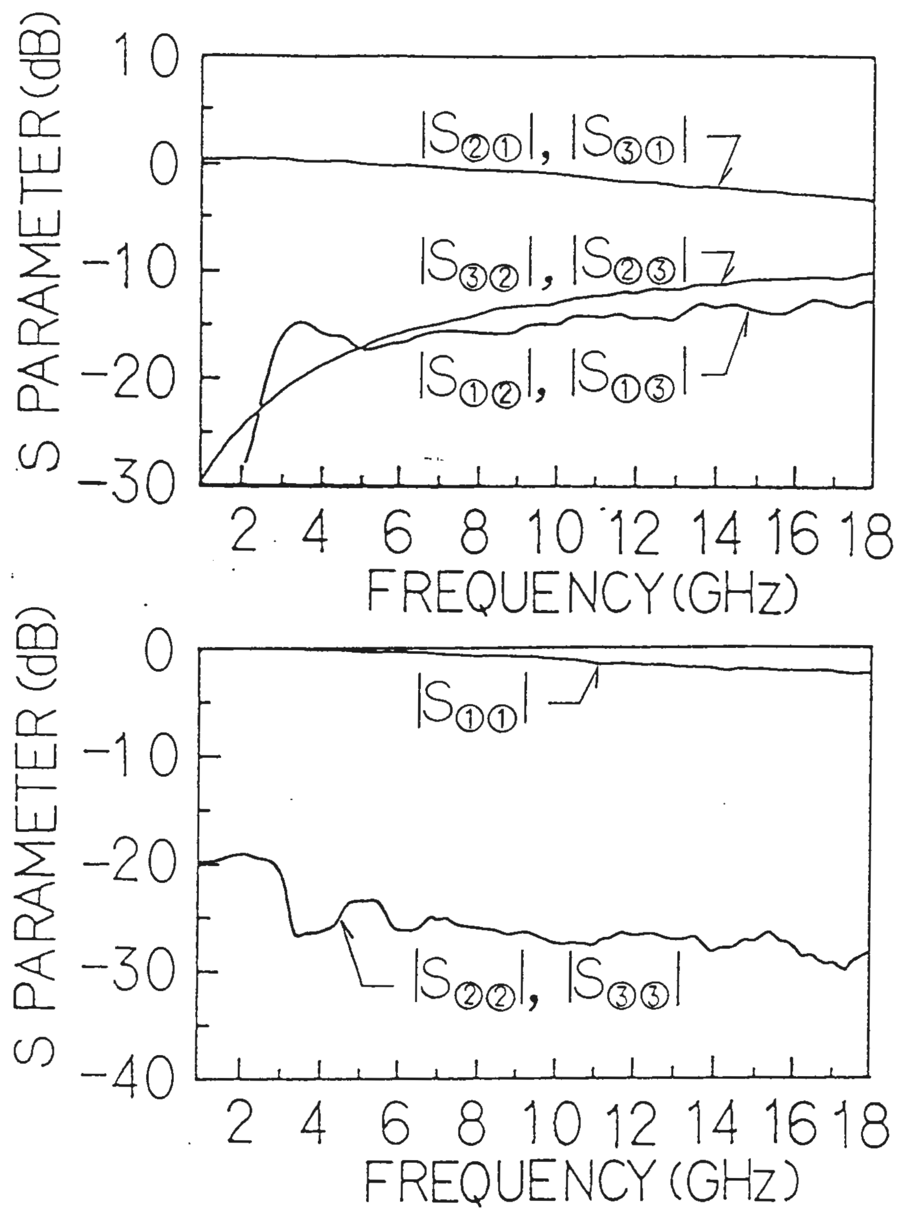


Fig. 2.4 S-parameters of the in-phase divider LUFET (e) measured between 1GHz and 18GHz.

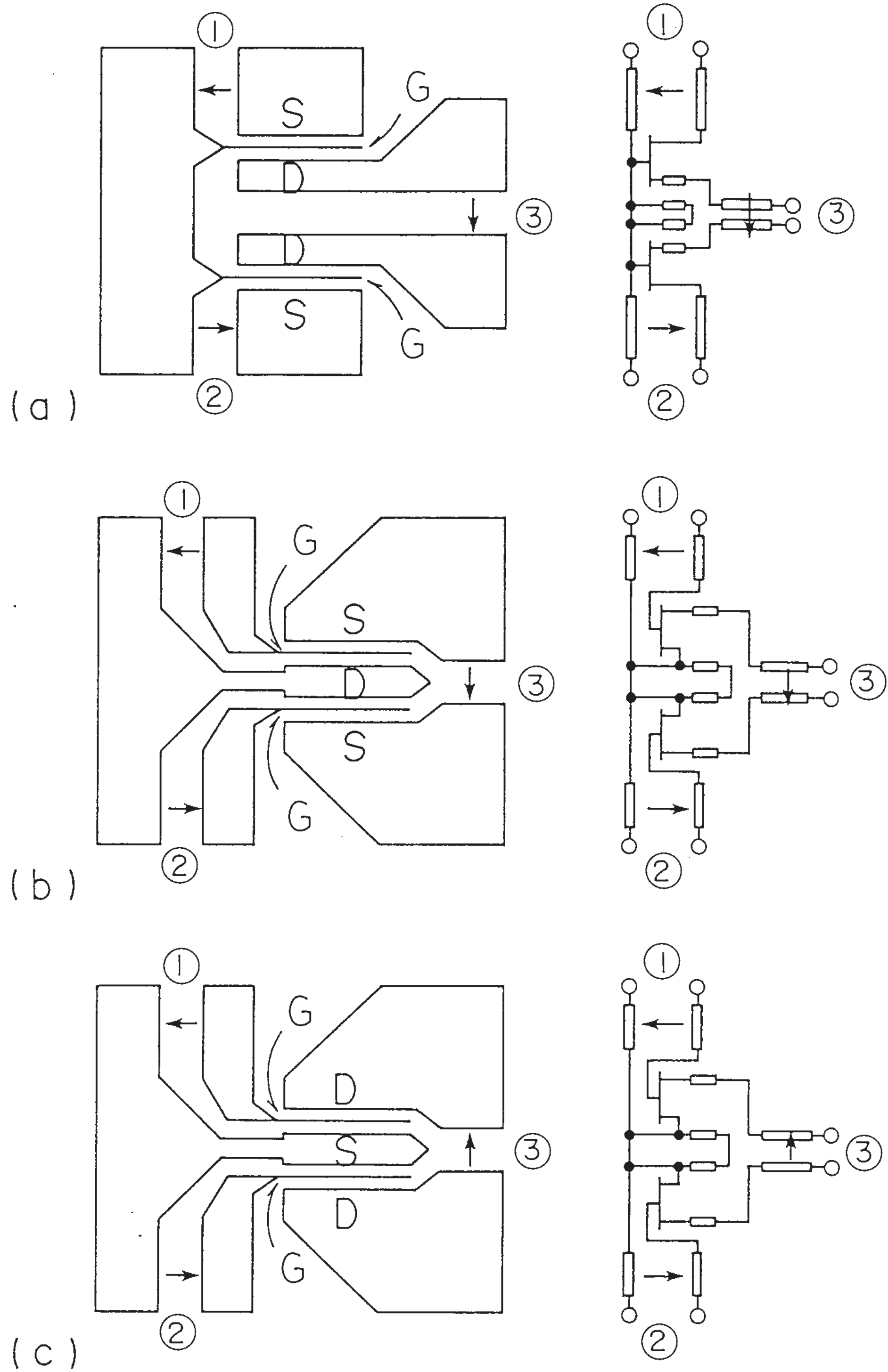


Fig. 2.5 Typical out-of-phase combiner and divider LUFETs and the equivalent circuit diagrams. (a)-(c) are combiner LUFETs and (d)-(f) divider LUFETs.

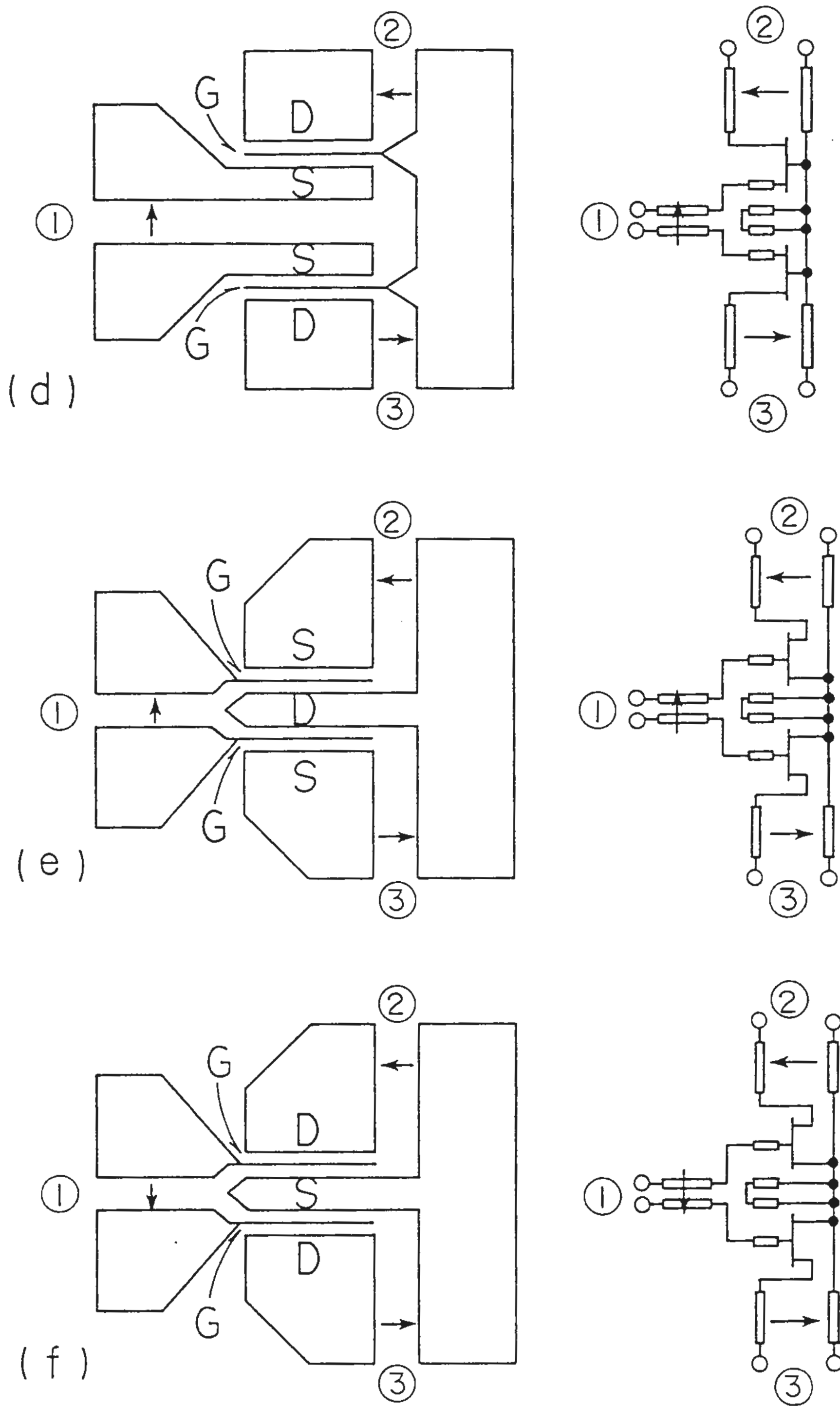


Fig. 2.5 Typical out-of-phase combiner and divider LUFETs and the equivalent circuit diagrams. (a)-(c) are combiner LUFETs and (d)-(f) divider LUFETs.

Table II
Coupling gain of out-of-phase combiner and divider LUFETs

function / type	out-of-phase combiner	out-of-phase divider
common gate	(a) $\frac{g_m\sqrt{2Z_1Z_2}}{1+g_mZ_1}$ $(g_mZ_1=1)$	(d) $\frac{2g_m\sqrt{Z_1Z_2}}{2+g_mZ_1}$ $(g_mZ_1=2)$
common drain	(b) $\frac{2g_m\sqrt{Z_1Z_2}}{2+g_mZ_2}$ $(g_mZ_2=2)$	(e) $\frac{g_m\sqrt{2Z_1Z_2}}{1+g_mZ_2}$ $(gmZ_2=1)$
common source	(c) $g_m\sqrt{2Z_1Z_2}$	(f) $g_m\sqrt{2Z_1Z_2}$

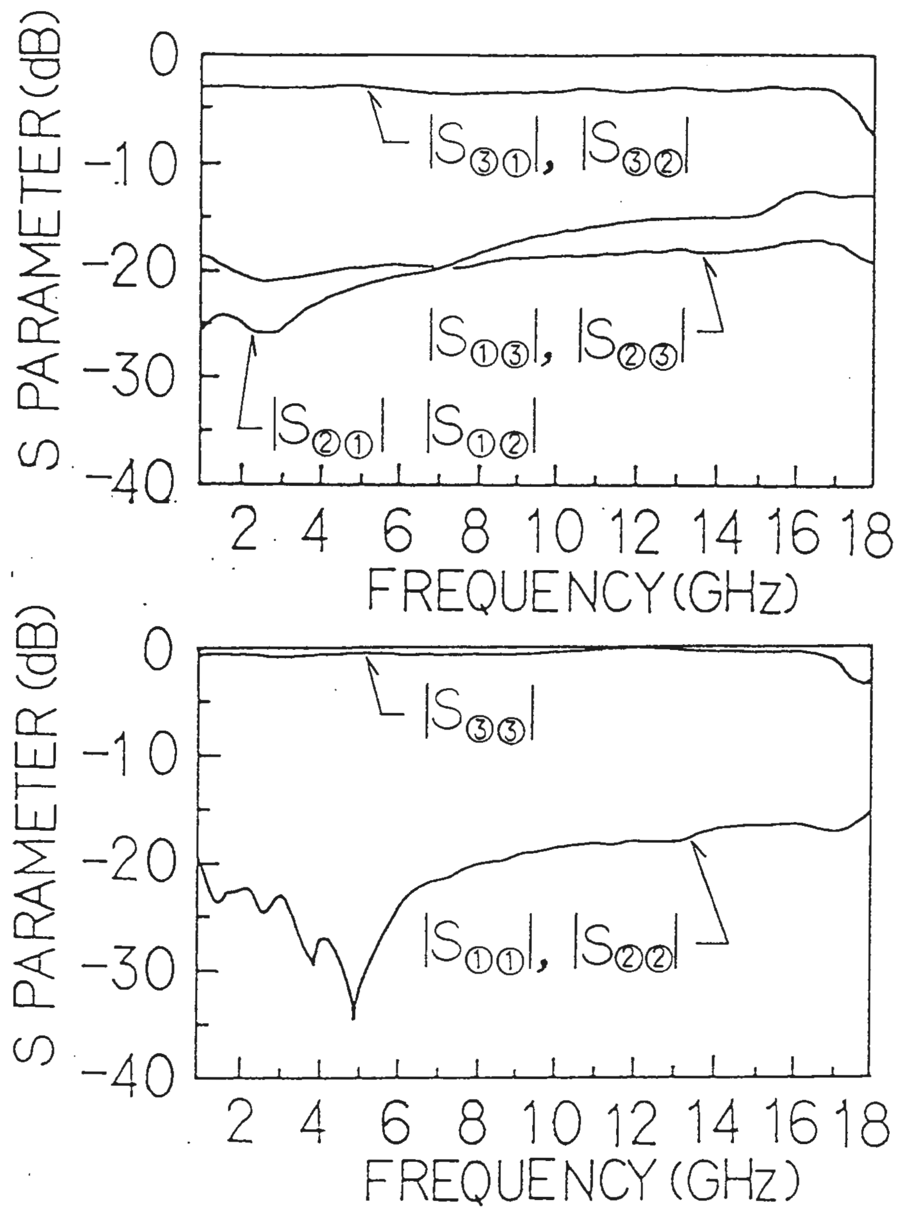


Fig. 2.6 S-parameters of the out-of-phase combiner LUFET (a) measured between 1GHz and 18GHz.

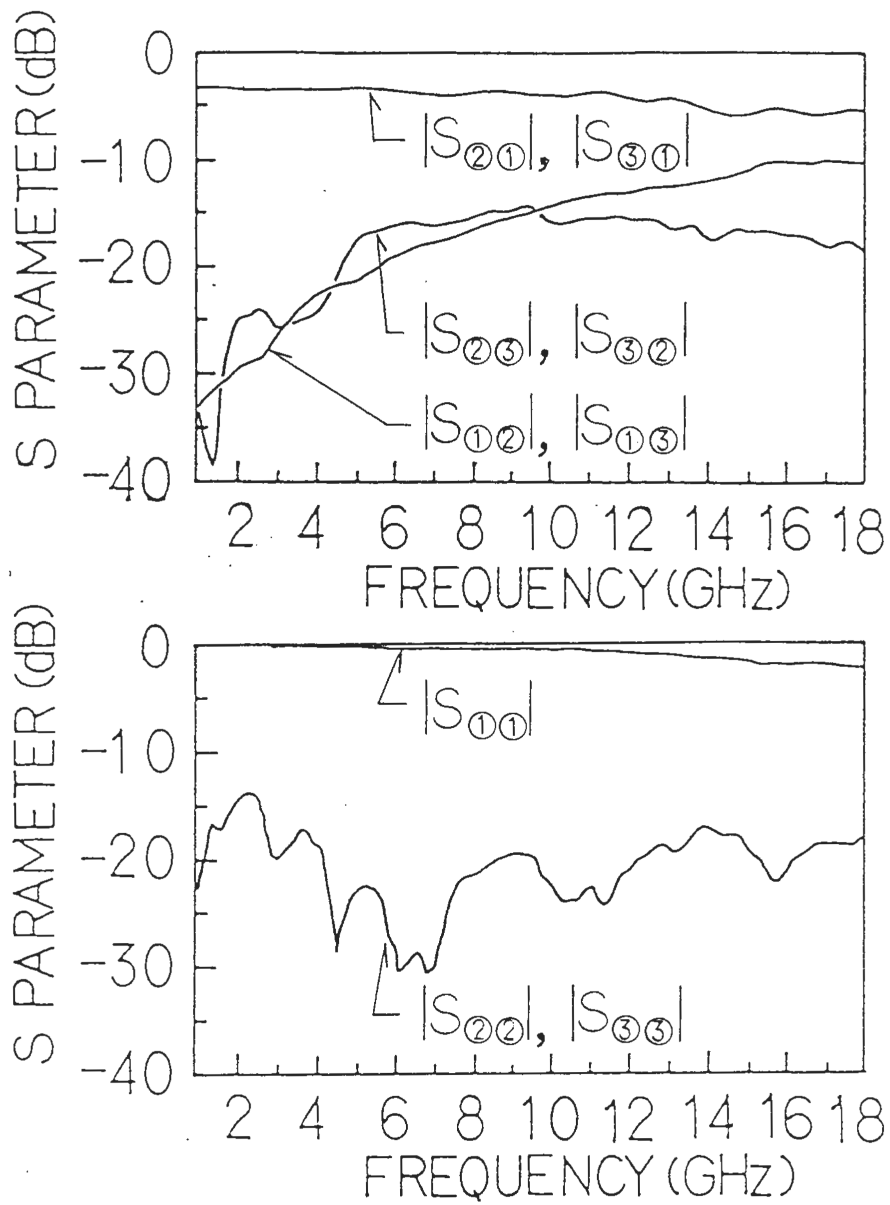
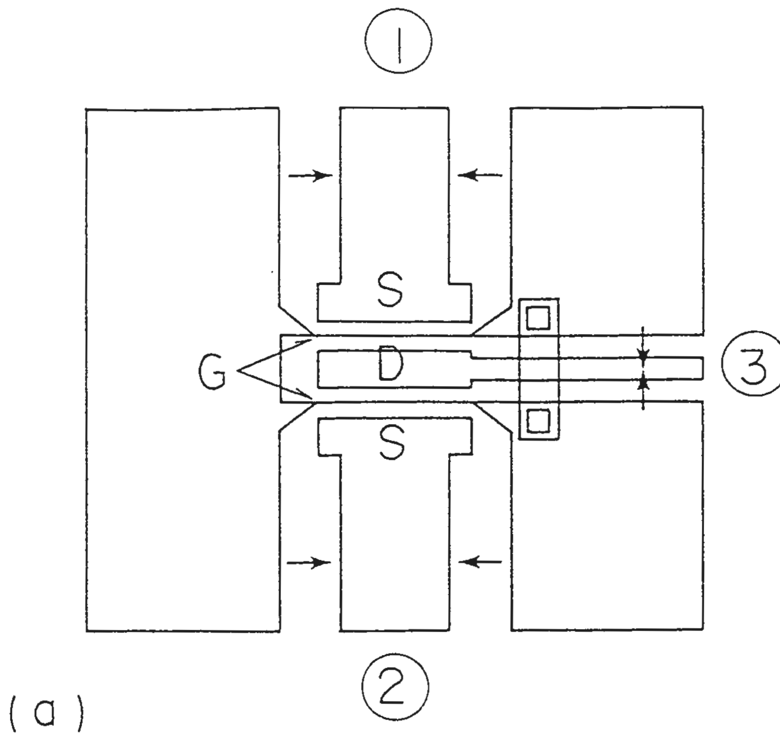


Fig. 2.7 S-parameters of the out-of-phase divider LUFET (e) measured between 1GHz and 18GHz.



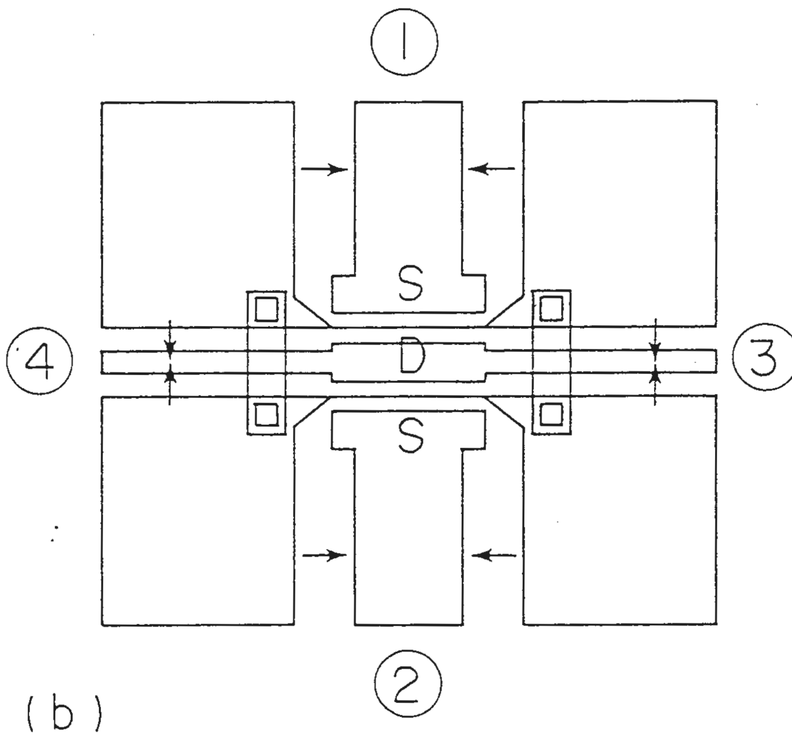


Fig. 2.8 Extended combiner LUFETs. (a) LUFET with isolated CPW input ports. (b) LUFET with isolated CPW input ports and signal-through CPW output ports.

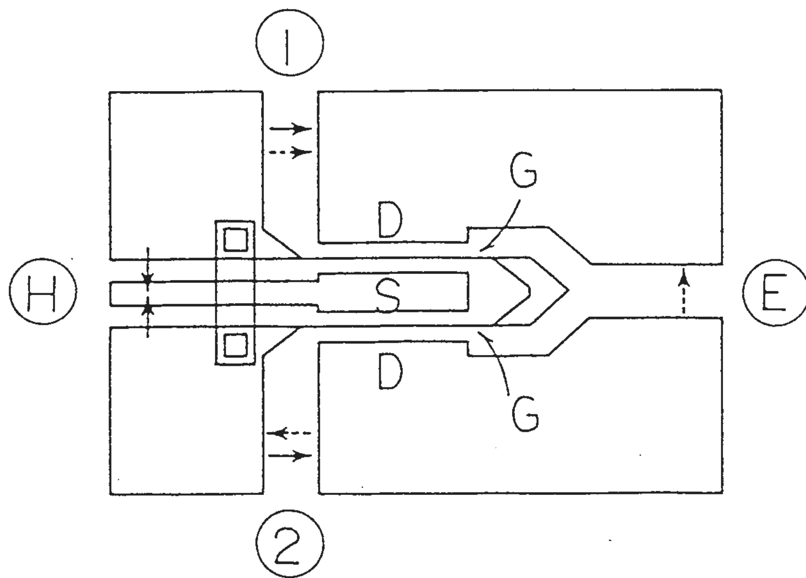


Fig. 2.9 Sophisticated, 1-18 GHz magic T LUFET derived from the in-phase divider LUFET shown in Fig. 2 (d). The area occupied by a magic T LUFET is less than 0.15mm^2.

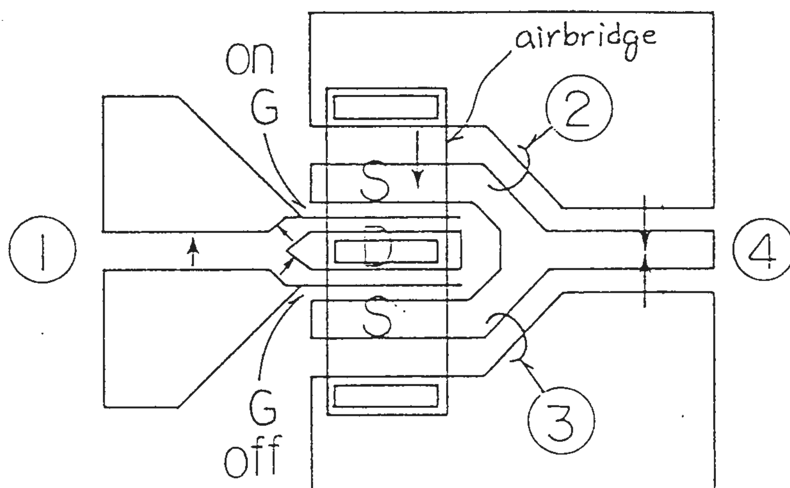


Fig. 2.10 Configuration of a sophisticated, phase inverter LUFET derived from the out-of-phase divider LUFET shown in Fig. 5 (f). The size of an implemented phase inverter LUFET is 0.6mm × 0.5mm.

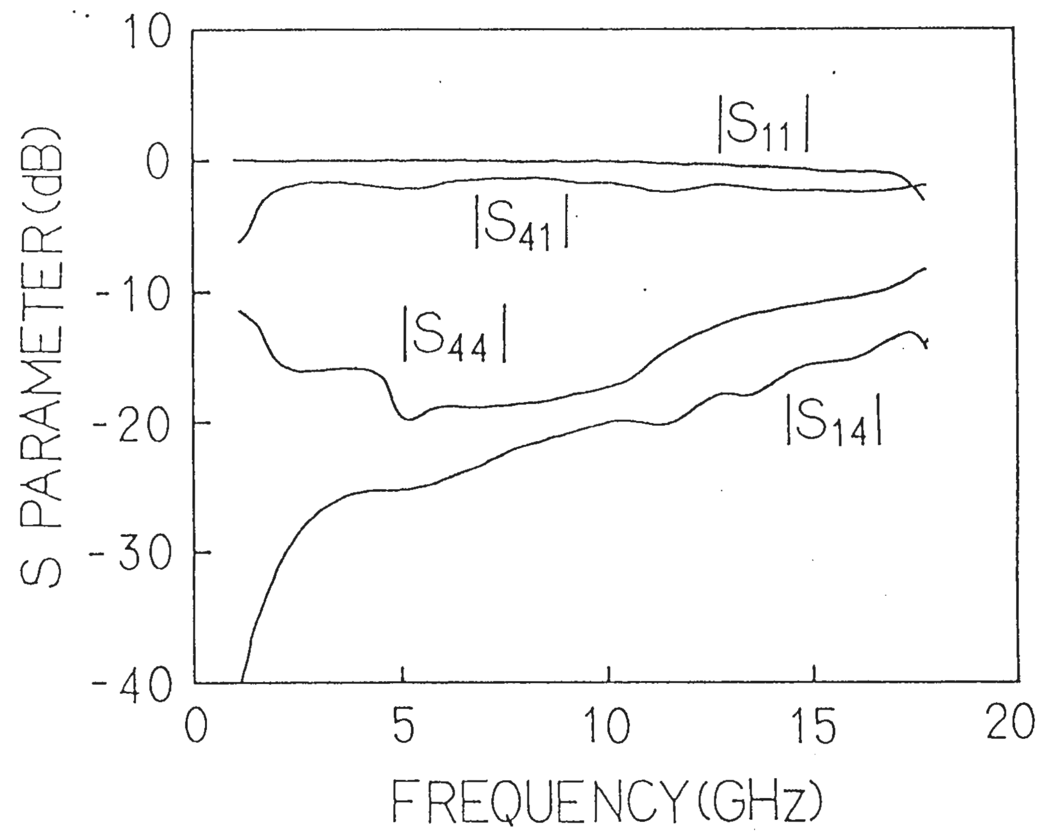


Fig. 2.11 Measured performance of the phase inverter LUFET.

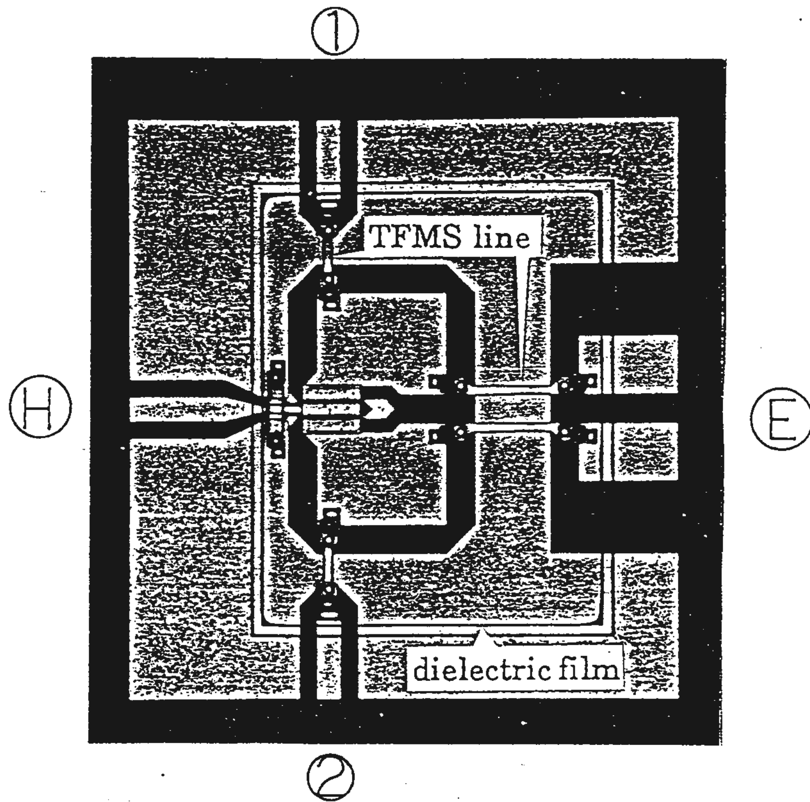
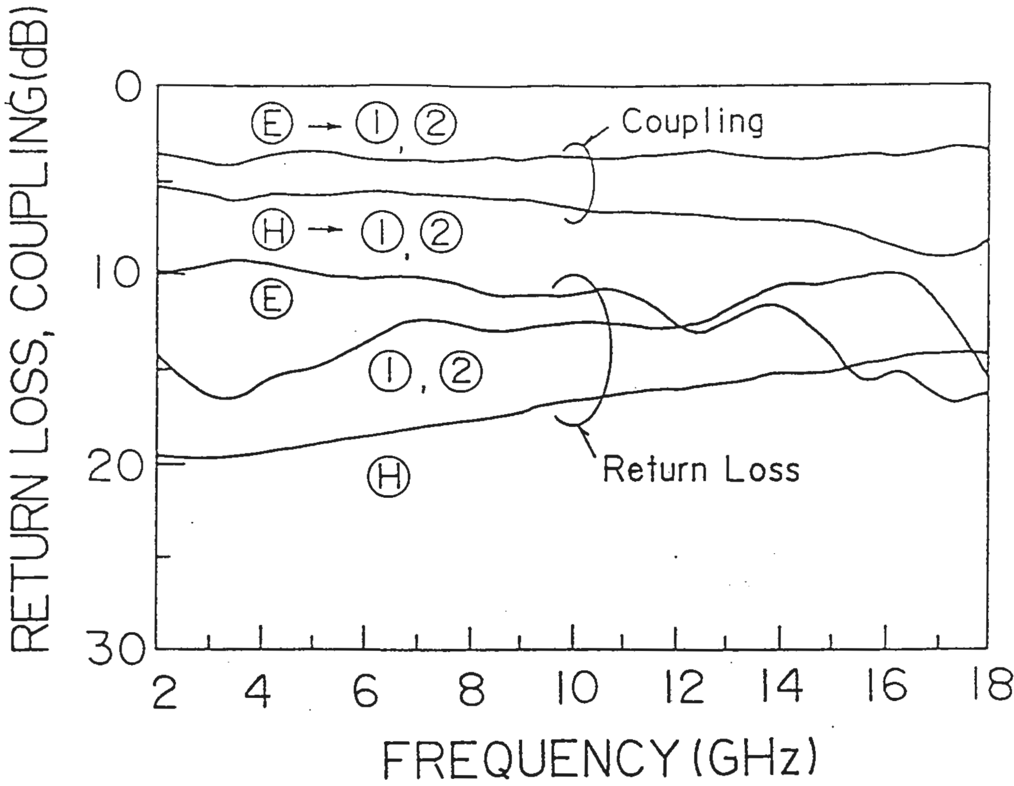


Fig. 2.12 Photograph of a magic T MMIC surrounded by a ground. The chip size is 1mm×1mm, and the intrinsic area covered by the dielectric film is 0.45mm^2.



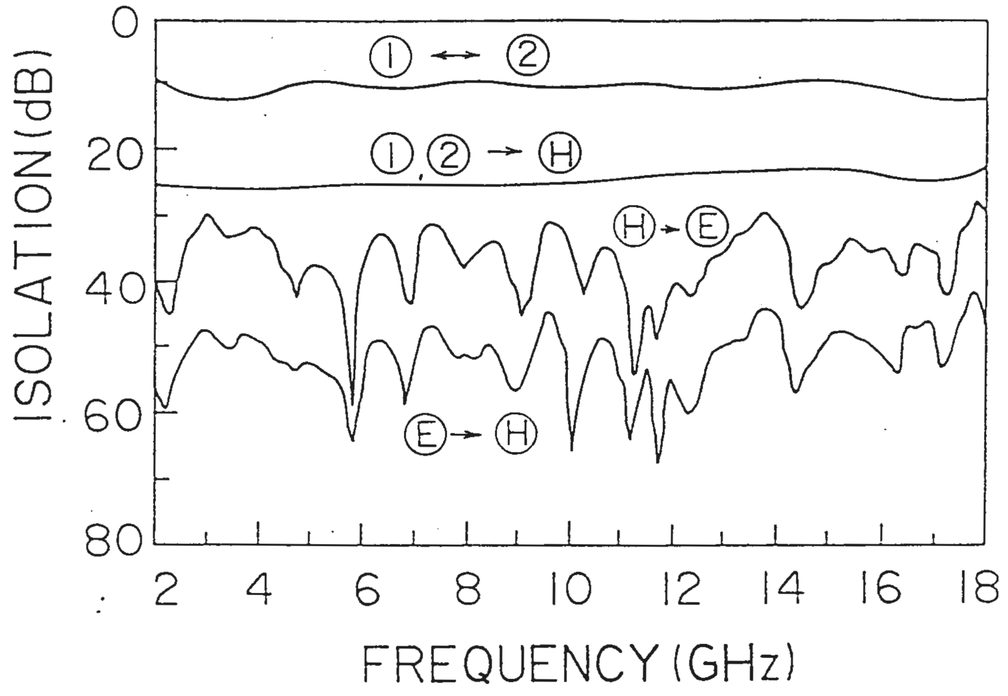


Fig. 2.13. Measured performance of the magic T MMIC surrounded by a ground.

2.3. マジック T LUFET
2.3. Magic T LUFET

An FET-size, 1-18GHz MMIC magic-T (180° hybrid) which unifies two different dividers, electrically isolated from each other, in a novel GaAs FET electrode configuration based on the "LUFET" concept, is demonstrated through an analysis and experiment.

In this section, a very simple, monolithic active magic-T, which has been shown in the previous section, is described in detail. The most significant innovation of the magic-T is a novel circuit structure which effectively uses a two-gate GaAs FET to unify two different dividers within the electrode configuration. An advantage of the proposed magic-T LUFET is that it remarkably reduces MMIC chip size, as well as operates in an ultra-wideband, due to the minimum use of GaAs FETs and the absence of spiral inductors. Such a miniaturized and wideband magic-T allows applications to many MMICs for RF signal processing (see paragraphs 2.4.4 and 2.4.5).

2.3.1. 構成と動作
2.3.1. Configuration and Design

The schematic and equivalent circuit of the proposed magic-T is shown in Fig. 2.14. The active magic-T is composed of a two-gate GaAs FET and coplanar transmission lines unified within the electrode locations of drain-gate-source-gate-drain. An in-phase power divider, with the coplanar waveguide input port Ⓗ and slotline output ports ① and ② electrically isolated from one another, is realized by the electrode allocation, where the gates serve as the module's common electrode. Furthermore, a slotline series T-junction as an out-of-phase power divider, with the slotline input port Ⓔ and the slotline output ports ① and ②, is formed with a conductive pad connecting the two gate electrodes and two drain electrodes, one on each side of the pad. In other words, two different

dividers are unified in the GaAs FET electrode locations, while the two dividers are isolated from each other because of the orthogonal mode effect and the unilateral effect of the GaAs FET. The impedance match at port Ⓗ is determined by the transconductance of the two-gate GaAs FET. The impedance at the other ports and the isolation characteristics between ports ① and ② are determined by the slotline T junction and the equivalent resistance between the drain and the gate of each GaAs FET.

This magic-T operates in an ultra-wideband frequency range because the parasitics in the GaAs FETs are terminated with low impedance Zo and because of the absence of frequency-dependent circuitry such as quarter-wavelength transmission lines and spiral inductors. The two dividers, the in-phase power divider and the out-of-phase power divider, are separated as shown in Fig. 2.15. R_{DG} is the equivalent resistance observed or connected between the drain and the gate of each GaAs FET. The in-phase power divider analysis gives the reflection coefficient $S_{ⒽⒽ}$ at port Ⓗ and power coupling $|S_{①Ⓗ}|$, $|S_{②Ⓗ}|$ from port Ⓗ to ports ① and ② as shown in equation (1) and (2).

$$S_{ⒽⒽ} = \frac{1-2g_m Z_{OH}}{1+2g_m Z_{OH}} \qquad (2.1)$$

$$|S_{①Ⓗ}| = |S_{②Ⓗ}| = \frac{2g_m\sqrt{Z_{OH}Z_0}}{1+2g_m Z_{OH}} \cdot \frac{R_{DG}}{R_{DG}+Z_0} \qquad (2.2)$$

where, g_m is the transconductance of each common gate GaAs FET. The isolation from ports ① and ② to port Ⓗ is due to the unilateral characteristic of each GaAs FET. The reflection coefficient $|S_{ⒽⒽ}|$ is at its minimum, that is zero, when $2g_mZ_o=1$, while the power coupling $|S_{①Ⓗ}|$, $|S_{②Ⓗ}|$ is about -6dB. The out-of-phase divider analysis, as shown in Fig. 2.16, through an orthogonal mode analysis based on the symmetrical configuration of the slotline series T junction yields the following equations giving the reflection coefficient $|S_{①①}|$, $|S_{②②}|$,

$|S_{ⒺⒺ}|$ at ports ①, ② and Ⓔ, the isolation $|S_{①②}|$, $|S_{②①}|$ between ports ① and ②, and the power coupling $|S_{①Ⓔ}|$, $|S_{②Ⓔ}|$, $|S_{Ⓔ①}|$, $|S_{Ⓔ②}|$ between ports ① or ② and port Ⓔ.

$$|S_{①①}|=|S_{②②}|=\frac{|\Gamma_{+-}+\Gamma_{++}|}{2} \qquad (2.3)$$

$$|S_{①②}|=|S_{②①}|=\frac{|\Gamma_{+-}-\Gamma_{++}|}{2} \qquad (2.4)$$

$$|S_{ⒺⒺ}|=|\Gamma_{+-}| \qquad (2.5)$$

$$|S_{①Ⓔ}|=|S_{②Ⓔ}|=|S_{Ⓔ①}|=|S_{Ⓔ②}|$$

$$=\sqrt{\frac{1-|\Gamma_{+-}|^2}{2}}\cdot\frac{2R_{DG}}{2R_{DG}+Z_0} \qquad (2.6)$$

where, the reflection coefficient Γ_{+-}, Γ_{++} at port ① in each excitation mode is given by following equations.

$$Odd:\Gamma_{+-}=\frac{(Z_{OE}\parallel 2R_{DG})-2Z_0}{(Z_{OE}\parallel 2R_{DG})+2Z_0},\quad Even:\Gamma_{++}=\frac{R_{DG}-Z_0}{R_{DG}+Z_0}$$

The power coupling given by equation (6) is less than -3.5dB. The difference between the coupling given by equation (2) and (6) can be less than 2dB when $2gmZ_0$ is greater than 1.2. The resistor R_{DG} acts to reduce the reflection coefficient at ports ① and ②, and to increase the isolation between ports ① and ②.

2.3.2. 特性
2.3.2. Experimental Results

A photograph and the performance of the fabricated magic T are shown in Fig. 2.17 and Fig. 2.18, respectively. The chip size is 1mm×1mm×0.6mm, while the intrinsic area is only 300μm×400μm. This active magic T has been fabricated

using epitaxial growth 0.5μm gate length GaAs FETs with a cutoff frequency of approximately 20GHz. The unit gate width is 75μm.

The ultra-wideband characteristics of the magic T have been confirmed through on-wafer measurements up to 18 GHz as shown in Fig. 2.18. Drain bias V_d, 3V, for each drain electrode is supplied through the pads and MIM capacitors. Source bias, through a wideband bias T and an on-wafer-measurement probe attached at port Ⓗ, is adjusted for a transconductance better than 20mS. The typical current drawn is 10mA and power consumption is only 30mW, where I_{dss} of the 150μm gate width GaAs FET is between 30mA and 50mA. The measured performance (solid lines) is as follows: coupling loss from port Ⓗ or Ⓔ to ports ① and ② is within 5dB ± 1dB ; return loss at each port is greater than 10 dB; isolation is greater than 20 dB except between ports ① and ②, where it is about 10dB. The dashed lines in Fig. 2.18 show the calculated performance of the active magic T. The calculation is performed with a typical small-signal equivalent circuit of the GaAs FET and an R_{DG} value (700Ω) for both excitation modes. The reason the measured isolation between ports ① and ② is better than predicted, is believed to be due to the module's configuration. A spatial coupling, for example, between the coplanar waveguide and the slotlines separated by the gate electrodes, improves Γ_{++} thus improving the isolation. The spatial coupling occurs in only the even mode excitation, and reduces the equivalent resistance R_{DG} for this mode. Isolation between ports ① and ② is improved by 2dB when isolation from ports ① and ② to portⒽ is about 25dB as shown in Fig. 2.18. Thus, the equivalent resistance R_{DG} in each excitation mode should be estimated individually for more accurate design.

The magic T LUFET can be applied to miniaturized, wideband balanced mixers. Fig. 2.19 shows the output power versus input power characteristics of the magic T, where two power-incident ports Ⓗ and Ⓔ are examined. The characteristic from port Ⓔ to port ① exhibits good linearity up to 18 dBm input power or more, while that from portⒽ to port ① begins a gain compression near 5

dBm input power. Thus, LO power from portⒺ can be sufficiently high to achieve low conversion loss.

Additionally, the magic T LUFET can change itself to another LUFET merely by interchanging the supplied voltages, due to electrode locations change from drain-gate-source-gate-drain to source-gate-drain-gate-source. This LUFET operates as a mode splitter, where in-phase signals and out-of-phase signals from ports ① and ② emerge at portⒽ and at portⒺ respectively, with an insertion loss of about 3dB for each.

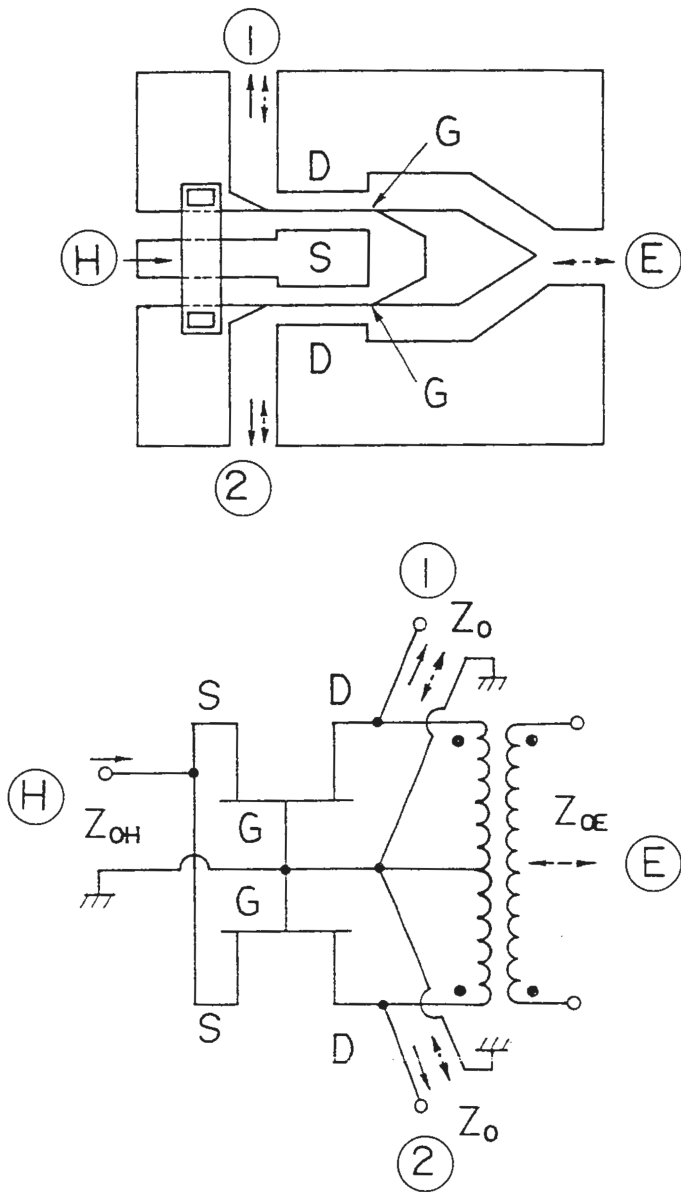
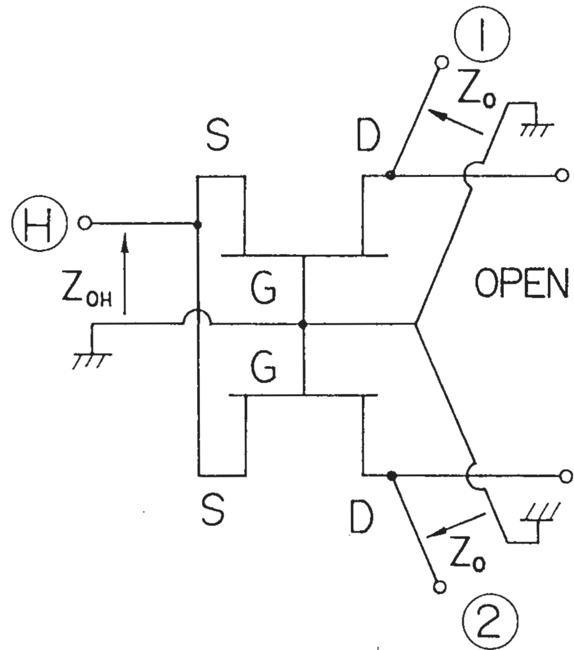
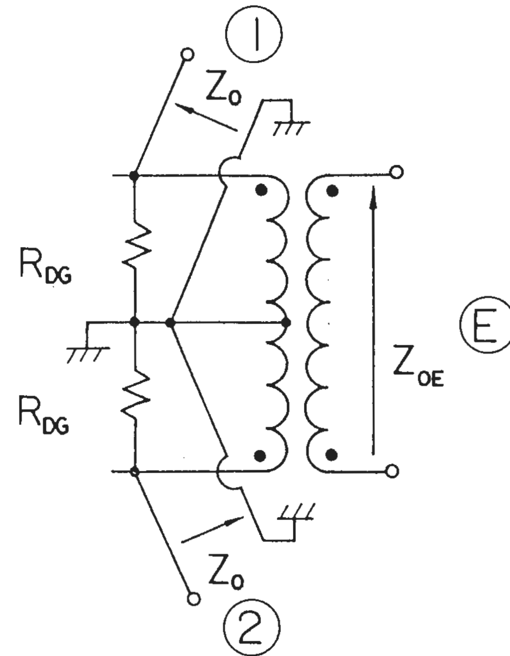


Fig. 2.14 Configuration and Equivalent Circuit Diagram of the Magic T LUFET.



(a) in-phase power divider



(b) out-of-phase power divider

Fig. 2.15 Two Dividers Unified in the Magic-T Configuration.

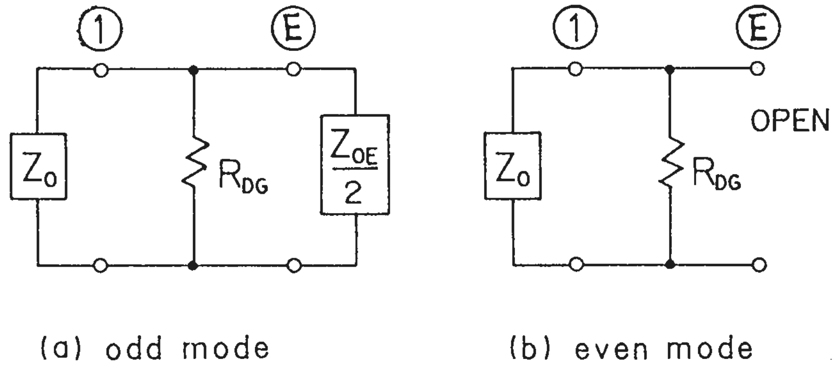


Fig. 2.16 Orthogonal Mode Analysis of the Out-of-Phase Power Divider.

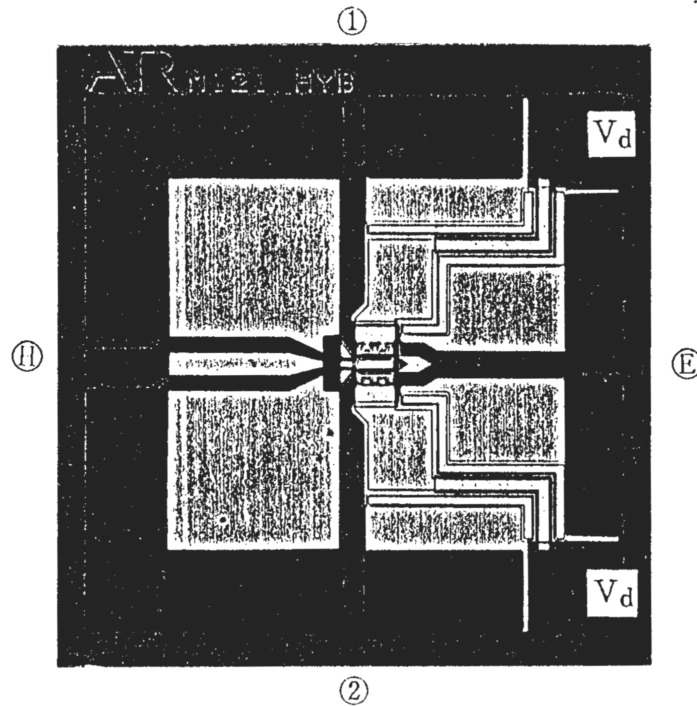


Fig. 2.17 Photograph of the Magic-T LUFET on a 1mm x 1mm Chip (Intrinsic Area is Only 0.15mm x 0.25mm).

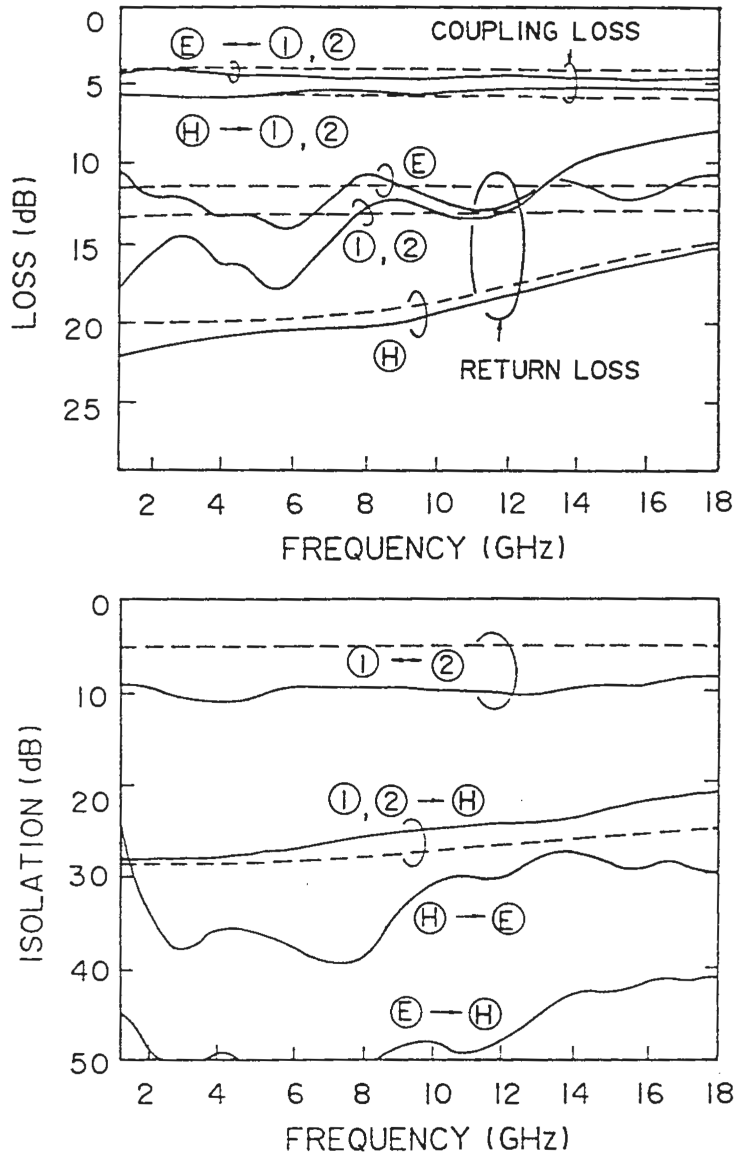


Fig. 2.18 Performance of the Magic-T LUFET (Solid Line: Measured, Dashed Line: Predicted).

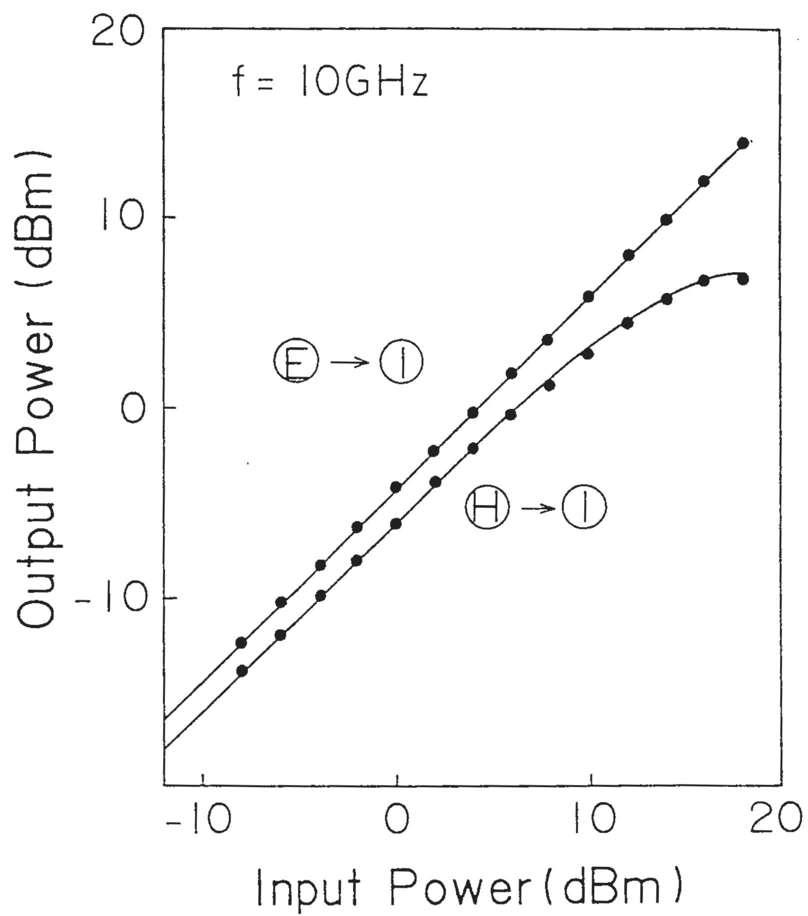


Fig. 2.19 Output Power versus Input Power Characteristics of the Magic T LUFET.

2.4. LUFETを用いた超小型MMIC
2.4. LUFET Application to Miniature MMICs

LUFET application to RF signal processing elements such as multiport combiner/dividers, mixers, balanced modulators, signal path switches and circulators are proposed and demonstrated. These MMICs are realized by modifying and combining LUFETs. The area of fabricated LUFETs and LUFET MMICs is between 0.1mm^2 and 1.5mm^2, and the average is about 0.5mm^2. Multi-octave-band operations suitable for generic use are also easily achieved.

In multifunction and RF signal processing MMICs, many non-amplifier circuits are required. These must be very small to be implemented on a reasonably small MMIC chip in a higher level of operation. The main circuit functions required in such MMICs are multiport dividing/combining and switching, mixing, phase and level control, filtering, etc.. Recently, compact non-amplifier MMICs such as N×M passive switches [2.14], non-blocking active 2×2 switches [2.15], double balanced mixers with active baluns [2.3] and transversal filters [2.16]have been reported. These MMICs are based on series and shunt switching FET conbination and distributed amplifier architecture. When non-reciprocal characteristics are required, the distributed amplifier architecture is mainly used. This architecture is certainly general-purpose. However, the relatively large circuit configuration and extensive use of FETs and inductive lines could obstruct a higher level of integration.

We propose and demonstrate LUFET applications for multifunction monolithic microwave circuits. LUFETs are microwave "circuit function modules" as described in sections 2.1 and 2.2. By including various circuit functions in the LUFET configuration, as well as by combining LUFETs, MMICs can be simplified and miniaturized. In this section, we describe our design approach and the results achieved with the newly developed LUFETs and the active matching technique. First, a 2×1 combiner MMIC using an in-phase combiner LUFET, and N×N combiner/divider based on the 2×1 combiner

topology are presented. Second, a single-end mixer and balanced mixer implemented by combining divider and combiner LUFETs are presented, where a balanced mixer LUFET is proposed. Third, a balanced modulator which is realized by slightly changing the phase inverter LUFET configuration is presented. This modulator is also a LUFET. Fourth, a signal path switch with a configuration of symmetrically combined magic T LUFETs and application to a 4×4 switch matrix are presented. Finally, a circulator which is a combination of in-phase and out-of phase, divider and combiner LUFETs, is presented. These function blocks, as well as the LUFETs in sections 2.2 and 2.3, have been fabricated using epitaxial growth and ion-implanted 0.5μm gate length GaAs FETs with a gate width of between 75μm and 200μm and a cutoff frequency fT of approximately 20GHz. The saturation power of the 150μm gate width GaAs FET is, as shown in Fig. 2.20, greater than 13dBm, and the gain linearity is maintained up to 7dBm of output power for CSF and 13dBm of output power for CGF and CDF.

2.4.1 分配·合成器
2.4.1.Combiner and Divider

A. 2×1 Combiner

A photograph and equivalent circuit diagram of a 2×1 combiner MMIC using the LUFET are shown in Fig. 2.21 [2.9]. The chip size is 1mm×1.1mm. The area enclosed in the dashed line is an in-phase, common gate combiner LUFET. This combiner, which is impedance matched at the input ports due to the common gate LUFET, includes a common drain FET for output impedance match. In this function block, the resistor R is used for determining the insertion gain G_i. When each port is actively impedance matched to Z_0 ($g_m Z_0 = 1$), G_i is given as follows:

$$G_i = [r(\omega)/2Z_0]\cdot[2g_m Z_0/1 + g_m Z_0]^2$$

$$= r(\omega)/2Z_0 \qquad \text{when } g_m Z_0 = 1 \qquad (2.7)$$

where r(ω) represents the equivalent shunt resistance between the CGF and CDF, and is designed so as to be nearly constant in the operating frequency region by using inductive elements to cancel the parasitic capacitance effects. Z_0 is the input and output impedance. Performance of the 2×1 combiner is as follows up to 10GHz: insertion loss is better than 13dB; isolation between inputs, and from output port to input ports is greater than 15dB and 25dB respectively. A 1×2 divider MMIC is designed and fabricated in similar fashion [2.9].

B. Multiport Combiner/Divider

Applying the extended combiner LUFET shown in section 2.2, as well as a similaly extended divider LUFET, to the above 2×1 combiner topology, multiport combiner/dividers can be miniaturized[2.17]. Figures 2.22 and 2.23 show a photograph and the equivalent circuit diagram of a 2×2 active combiner/divider MMIC. Advantages of this function block include broadband operation, as well as a simple configuration regardless of the number of ports. A six port cell which consists of an extended combiner LUFET, an extended divider LUFET, and a CR circuit, is connected with other cells as shown in the figure to provide the required number of isolated input- and output ports. A 3×3 combiner/divider is also implemented simply by adding another cell to the 2×2 combiner/divider. The combiner LUFET has a pair of isolated input ports ①, ② and a pair of signal-through output ports ③, ④. Conversely, the divider LUFET has a pair of signal-through input ports ①', ②' and a pair of isolated output ports ③', ④'. The input signal to each port ① is delivered to divider LUFETs through the corresponding combiner LUFET, drain electrode strips, and an LR circuit. Each CR circuit which connect ports ② and ③' offers a feedback loop to flatten the frequency response, independent of the above circuitry and port impedances because of the unilateral characteristics of the LUFETs.

The measured performance of 2×2 and 3×3 combiner/divider is shown in Fig. 2.24, where the same circuit parameters are used. The insertion loss of both combiner/divider is about 1dB, return loss is better than 15dB, and isolation among the input ports or output ports is greater than 20dB. Isolation from the output ports to the input ports is greater than 35dB. The chip size of the 2×2 combiner/divider is 1mm×1.4mm, and that of the 3×3 combiner/divider is 1mm×1.8mm.

When only one six-port cell is used with the LR circuit, this architecture provides an isolator MMIC with a chip size less than $1mm^2$. Fig. 2.25 shows the measured insertion loss vs. frequency characteristic (solid line) of the isolator, where the dashed line shows the characteristic calculated by omitting the feedback loop. As shown in Figures 2.25 and 2.24, the feedback circuit by the use of extended combiner and divider LUFETs is effective to flatten the frequency response.

2.4.2. 周波数変換器
2.4.2. Mixer

A. Lossless Combiner and Mixer

A photograph and equivalent circuit diagram of a mixer are shown in Fig. 2.26. The chip size is 0.9mm×1.4mm. This mixer contains a common gate, in-phase combiner LUFET and a miniaturized broadband amplifier module [2.18] which are joined together through replacing the input common gate GaAs FET (CGF) in th original amplifier module with the combiner LUFET. Inductors L1 and L2 are used to compensate for bandwidth degradation due to parasitics in the FETs, and to provide a frequency-independent constant signal voltage between the CSF gate and source. This MMIC in a linear state operates as a combiner with some insertion gain as shown in Fig. 2.27, where a lossless characteristic up

to 11GHz is obtained. When the CSF is dc-biased in a non-linear state, this MMIC operates as a mixer [2.19]. Voltage conversion gain $G_M(\omega)$ of this mixer, as a function of frequency ω, can be estimated using eq. (8). This is derived from the Curtice model [2.20]. The details of the calculation of $G_M(\omega)$ are explicitly given in the Appendix. A simplified equivalent circuit diagram for the calculation is shown in Fig. 2.28, where $Z_{l1}(\omega)$ and $Z_{l2}(\omega)$ are equivalent load impedances for the FETs.

$$G_M(\omega) \simeq G_C(\omega) \cdot (I_{dss}/2g_m V_p^2) \cdot |v_{LO}(\omega)| \qquad (2.8)$$

where $G_C(\omega)$ is the voltage insertion gain in the linear state and I_{dss}, V_p are saturated dc drain current at zero gate bias, pinch-off voltage of the GaAs FET biased in a nonnlinear state respectively. $|v_{LO}(\omega)|$ is the voltage across the GaAs FET gate and source. Transconductance g_m in the linear state is assumed to be constant over the pinch-off voltage. $G_M(\omega)$ is nearly proportional to $G_C(\omega)$ because $|v_{LO}(\omega)|$ is nearly constant over the operating frequency region. Fig. 2.29 shows the measured conversion loss when the MMIC is used for down-converter and up-converter, where the common source GaAs FET (CSF) is biased in a nonlinear state. At RF signal frequencies between 3GHz and 10GHz, a conversion loss of 5dB$\pm$2dB and 2dB$\pm$2dB are obtained for down- and up converters, respectively, with return loss better than 15dB. The noise figure of this mixer is about 12dB.

B. Balanced Mixer

Configuration of a balanced mixer LUFET is shown in Fig. 2.30 [2.21]. This LUFET is constructed using a 4-gate GaAs FET with S_{LO}-G_{LO}-D-G_{RF}-S_{RF}-G_{RF}-D-G_{LO}-S_{LO} electrode locations, a conductive pad M_G connecting G_{LO}s, and coplanar lines within the electrode locations. An in-phase divider, out-of-phase divider, and in-phase combiners are unified in the electrode locations by an airbridge connecting the gate electrode strips used as common electrode. The in-

phase divider which is formed by the D-G_{RF}-S_{RF}-G_{RF}-D structure and port Ⓗ, corresponds to an in-phase, common gate divider LUFET. The in-phase combiner which is formed by the S_{LO}-G_{LO}-D-G_{RF}-S_{RF} structure and port ① or ② derived from the drain electrode D through a thin film microstrip (TFMS) line [2.12-2.13], corresponds to an in-phase, common gate combiner LUFET. The divider which is out-of-phase is a slotline T junction with port Ⓔ, and is formed with the conductive pad M_G and two source electrodes one on each side of the pad. The two branches are fed to the in-phase combiners. The TFMS lines are fabricated using 9μm SiON film deposited on the electrodes and GaAs substrate surface. This TFMS line can be effectively used to combine th IF ports beside the LUFET.

When ports Ⓗ and Ⓔ are used as RF input port and LO input port, respectively, and the in-phase divider is dc-biased in a non-linear state, this LUFET serves as a drain injection mixer module with impedance-matched input ports and high impedance output ports. The area occupied by this LUFET is less than $0.3mm^2$. Figures 2.31 and 2.32 show a photograph and the equivalent circuit diagram of a balanced mixer MMIC. This MMIC is composed of a balanced mixer LUFET, TFMS lines, and output common drain FETs for output impedance matching. The chip size is $0.7mm \times 1.1mm$, and the intrinsic area after subtracting the input- and output-line area is $0.5mm \times 1.0mm$. Fig. 2.33 shows the measured conversion loss vs. frequency characteristic of the balanced mixer. This mixer MMIC exhibits the following performance between 8GHz and 20GHz: conversion loss is $8.5dB \pm 1.5dB$; return losses at the RF and LO input ports, and IF output port are between 8 and 18dB, and 8dB respectively; isolation between LO and RF ports is greater than 35dB; isolation between the IF and LO ports is greater than 30dB. The conversion loss increase at frequencies below 8GHz is due to the incomplete isolation between the LO and IF ports in the actual MMIC. A layout which complete the isolation is required for operation below 8GHz.

2.4.3. 平衡変調器
2.4.3. Balanced Modulator

Balanced modulators are easily implemented using a dual-gate phase inverter LUFET [2.22-2.23]. The configuration of a phase inverter LUFET shown in Part I is slightly changed from C-[S-G-D(C)-G-S]-C to C-[D-G_2-G_1-S(C)-G_1-G_2-D]-C, to control the output signal amplitude with the second-gate (G_2) dc voltage. G_1 indicates the first gate, and C the common electrode. A common source configuration is employed for a wide dynamic range. A photograph and the equivalent circuit diagram of the fabricated balanced modulator are shown in Fig. 2.34. The chip size is only 0.6mm×0.5mm. Two 1st gates and a source electrode form a slotline series T junction as an out-of-phase divider. The source electrode is connected to the outer conductor (C) of the output CPW by airbridges. Two drains are connected at the inner electrode of the CPW. Each second gate is used for the control of the output signal level. Each output from each FET is controlled by the 2nd gate voltage from some level P_0 to 0 and are out of phase with each other because the input signal is divided and input to each gate-source by the input slotline T junction, out of phase. Therefore, the output signal level can be continuously controlled from P_0 to $-P_0$.

Figures 2.35 and 2.36 show the measured performance of the balanced modulator MMIC. Fig. 14 shows variable gain characteristics. One 2nd gate bias is changed while the other 2nd gate bias is in the off state. Variable gain performance is obtained over a very broad band. Fig. 2.36 shows how the gain and impedances are changed by the second gate bias voltage at 10GHz. The gain is controlled from 0.7 to -0.7, while the input and output impedances do not change. Isolation is more than 35dB over all frequency points and at any bias point.

This type of LUFET MMIC is potentially a LUFET, that is, a balanced modulator LUFET. This extremely miniaturized, balanced modulator is effectively used in a vector-combiner-type, 1-chip 360°phase shifter together with a 90° hybrid and in-phase combiner LUFET. A multilayer-MMIC branchline coupler can, at present, be used in the 1-chip phase shifter due to its very small size less than $1mm^2$ [2.13, 2.22, 2.24].

2.4.4. 経路切替えスイッチ
2.4.4. Signal Path Switch

A photograph and equivalent circuit diagram of a signal path switch utilizing the magic T LUFET in Part I are shown in Fig. 2.37. The chip size is 1mm× 1mm, and the intrinsic area is 0.6mm×0.7mm. Two magic T LUFETs are combined symmetrically at ports ①, ② and Ⓔ. Slotlines of the LUFETs are coupled to provide CPW output ports ① and ②. The characteristics of this signal path switch and the magic T are represented in similar fashion because the only changes in the analysis equations [2.11] are equivalent impedance R_{DG} between the drain and gate to $R_{DG}/2$, and port Ⓔ impedance Z_0 to R_0. Therefore, signal power division from port H_1, H_2 to ports ① and ② is achieved maintaining port isolation in the magic T. Isolation between output ports ① and ② is significantly improved by increasing the R_0 value up to infinity.

This module can be used for signal path switching and simultaneous power dividing with good isolation, when the R_0 value is infinite or very large, by controlling the gate-source voltages for the two LUFETs. When the LUFET corresponding to port H_1 is in the on state and the other is in the off state, an input signal to port H_1 is delivered to ports ① and ② with a coupling loss of about 6dB, an H_1-to-H_2 isolation better than 20dB, a ①-② isolation better than 25dB,

and an H_2-to-①,② isolation better than 17dB, as shown in Fig. 2.38. In the opposite condition: the LUFET corresponding to port H_1 is in the off state and the other in the on state, the performance is given by only exchanging H_1 and H_2 in the above performance. Therefore, by mutually turning the LUFETs on and off, this module serves as a signal path switch. Use of dual gate FETs for the magic T LUFET should considerably improve the isolation characteristics.

This function block can be effectively used to miniaturize broadband N×M switches [2.11]. A 2×M switch, for example, consists of M signal path switches which are connected to one of two input lines at port H_1 and to the other input line at port H_2. Either port ① or ② of each signal path switch is the output port of the 2×M switch. An N×M switch is a combination of 2×M switches.

2.4.5. 4×4スイッチマトリクス
2.4.5. 4×4 Switch Matrix

Figure 2.39 shows a combination of two divider/combiner modules, i.e., a 4-port signal combiner. The square represents the switch (divider/combiner) module in Fig. 2.37, where the triangle which suggests directivity represents the two-gate GaAs FET, and the dot in a circle represents the slotline-CPW T junction. This circuit combines 4 input signals A, B, C, and D, when all FETs are in the on-state, indicated by black triangles in the illustration. In addition to this output, i.e., (A+B+C+D)/2, other outputs such as (A+B)/2 and (C+D)/2 are also available. The symbol ∞ (infinity) means that the Ro value is infinite, and isolation between ports ① and ② is sufficiently complete as shown in Fig. 2.38, and the impedance of ports ① and ② is very high compared with load impedance Zo. Therefore, the above three outputs are independent of each other. This circuit

is believed to be useful for vector combiners such as predistortors, phase shifters, and an adaptive linear combiner as the basic form of adaptive equalizer.

Figure 2.40 shows a 4x4 switch matrix utilizing 8 divider/combiner modules, where 4 circuits similar to that of Fig. 2.39 are cascaded. On-state GaAs FETs are represented by black triangles, off-state GaAs FETs by white triangles. When R_0 value and shunt impedance Z_i are infinite and Z_0 respectively, input signals A, B, C, and D emerge in the order B/2, A/2, D/2, and C/2 in the operation mode shown in Fig. 2.40. For every input signal only one of the areas indicated by a triangle (two-gate GaAs FET) is in the on-state. Thus, a good impedance match is obtained at every input port. The size of these application circuits can be effectively minimized due to the very small magic T LUFET, and by using a thin film microstrip (TFMS) line [2.12-2.13] and its cross-over structure.

2.4.6. サーキュレータ
2.4.6. Circulator

Fig. 2.41 shows a basic configurations of a quasi-circulator, where $S_{21}=S_{32}=1$ and $S_{13}=0$ [2.25-2.26]. A unilateral out-of-phase divider LUFET and a unilateral in-phase combiner LUFET are connected. Port ② is branched from one of the connected lines, while shunt impedance Z_0 is connected to the other. The quasi-circulator realizes an isolation between ports ① and ③ due to the orthogonal mode effect. A signal from port ① is divided out of phase. The two signals to the in-phase combiner are out of phase, and equal in magnitude because the impedance of port ② and the shunt impedance Z_0 are equal. Therefore, the incident signal does not appear at port ③. On the other hand, S_{12}, S_{23}, and S_{13} are zero because of the unilateral characteristics of the the divider and combiner LUFETs. Another quasi-circulator using an in-phase divider

LUFET and out-of-phase combiner LUFET operates in similar fashion. The characteristics of the quasi-circulator is familiar in many circulator applications.

Figures 2.42 and 2.43 show a photograph of a quasi-circulator MMIC and its measured performance between 0.1GHz and 15GHz. The chip size is 0.6mm×0.5mm. This quasi-circulator is constructed based on Fig. 2.41, while the out-of-phase divider is a conventional FET divider composed of an FET, drain resistor, and source resistor. The insertion gain and directivity between 1GHz and 10GHz are: $|S_{21}|=|S_{31}|=-4.5\text{dB}\pm0.5\text{dB}$; $|S_{31}|$〈-15dB; $|S_{12}|$ and $|S_{23}|$〈-20dB; $|S_{13}|$〈-32dB. The return loss at port ② is better than 11dB in that frequency range. In this module, the isolation $|S_{31}|$ is not good in the high frequency range, because the out-of-phase performance of the out-of-phase divider degrades at high frequencies due to FET parasitic capacitances. The isolation will be improved considerably over the whole frequency range, by the use of an out-of-phase divider LUFET unifying a slotline series T junction.

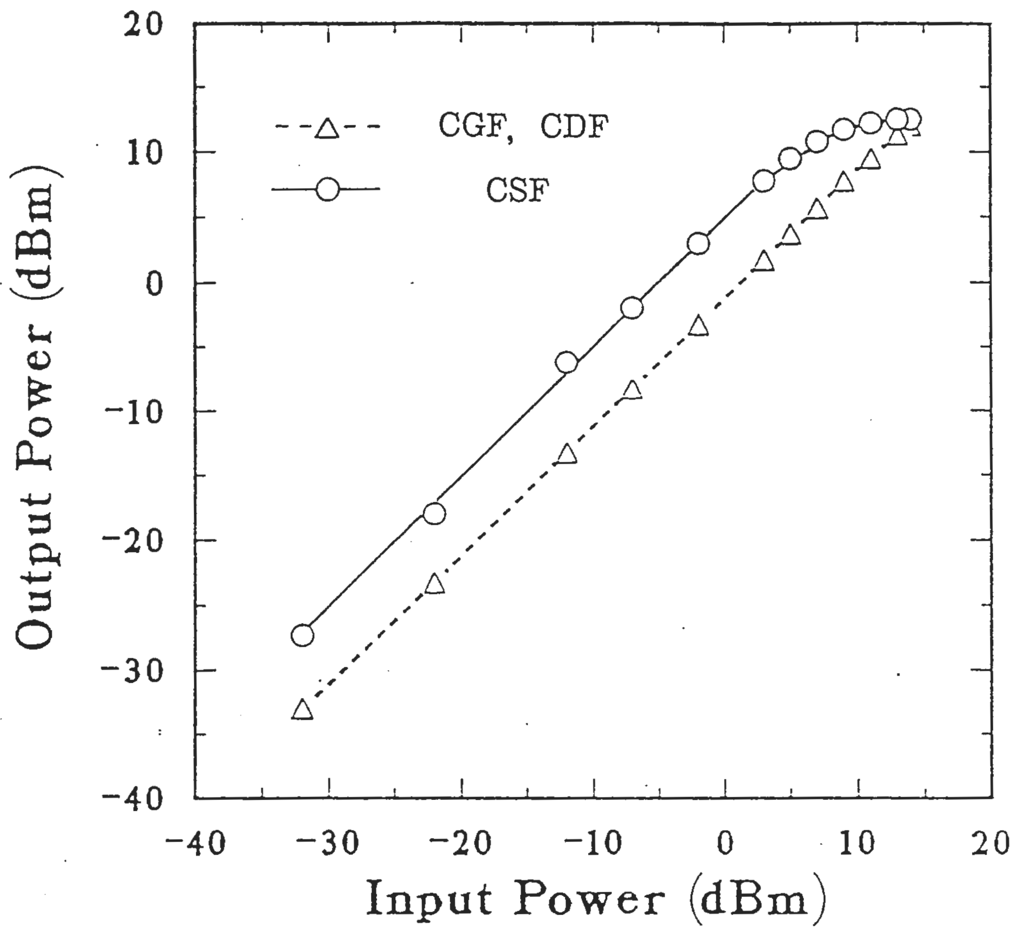


Fig. 2.20 単位LUFETの入出力電力特性(Wg＝150μm)

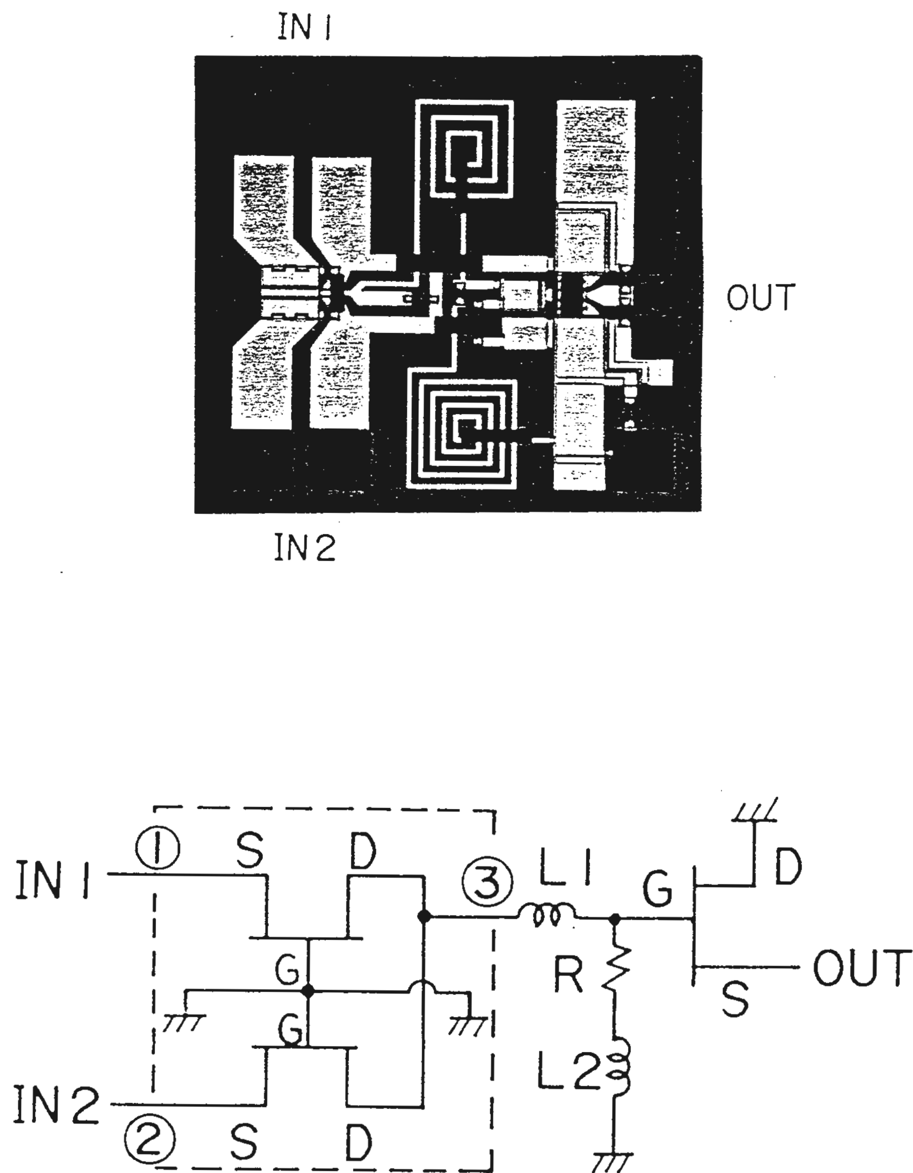


Fig. 2.21 Photograph and equivalent circuit diagram of a 2×1 combiner MMIC using the LUFET. The chip size is 1mm×1.1mm. The area enclosed by the dashed line is an in-phase, common gate combiner LUFET.

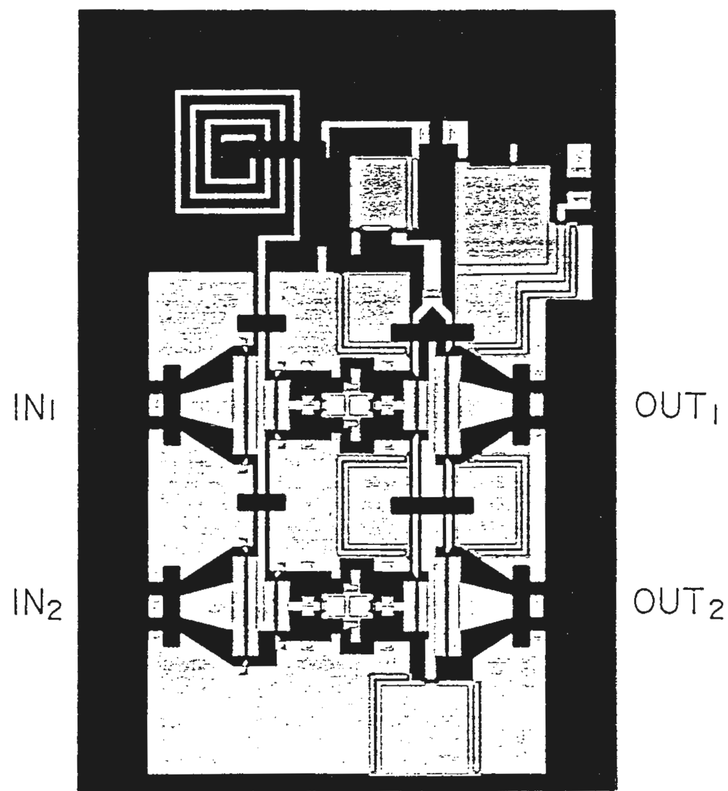


Fig. 2.22. Photograph of a 2×2 combiner/divider. The chip size is 1.0mm×1.4mm.

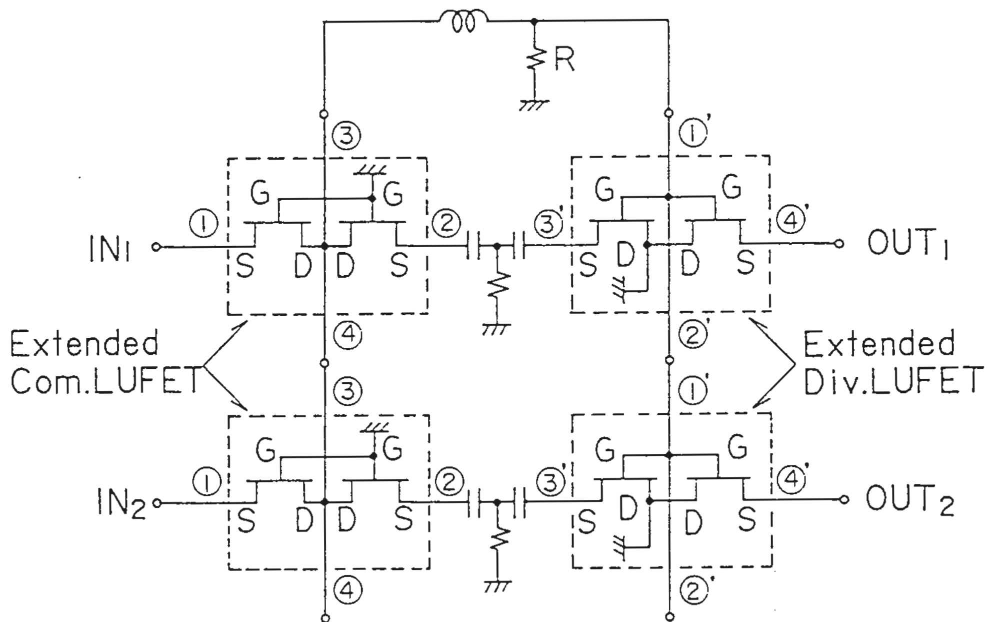


Fig. 2.23. Equivalent circuit diagram of the 2×2 combiner/divider, where two six-port cells are connected. The areas enclosed by the dashed line are extended combiner and divider LUFETs.

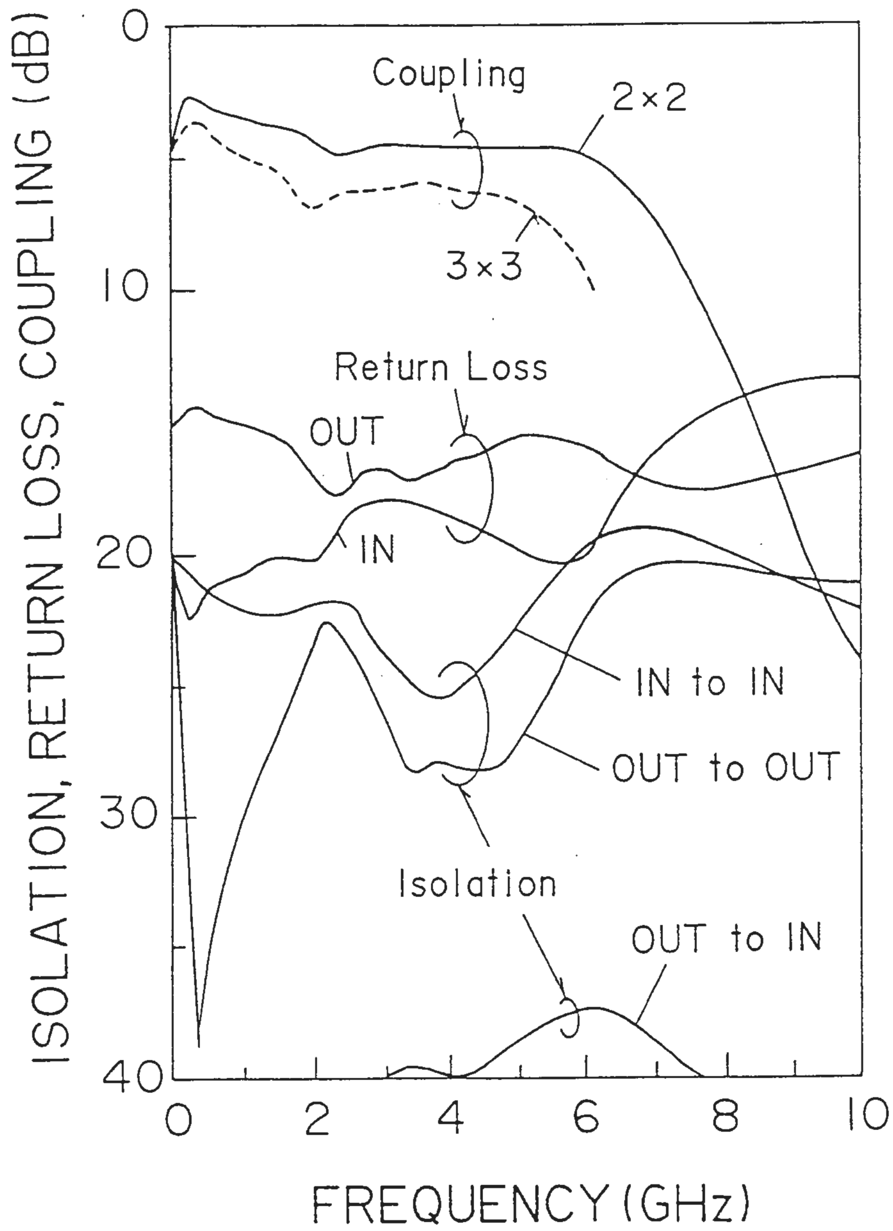


Fig. 2.24. Measured performance of 2×2 and 3×3 combiner/dividers.

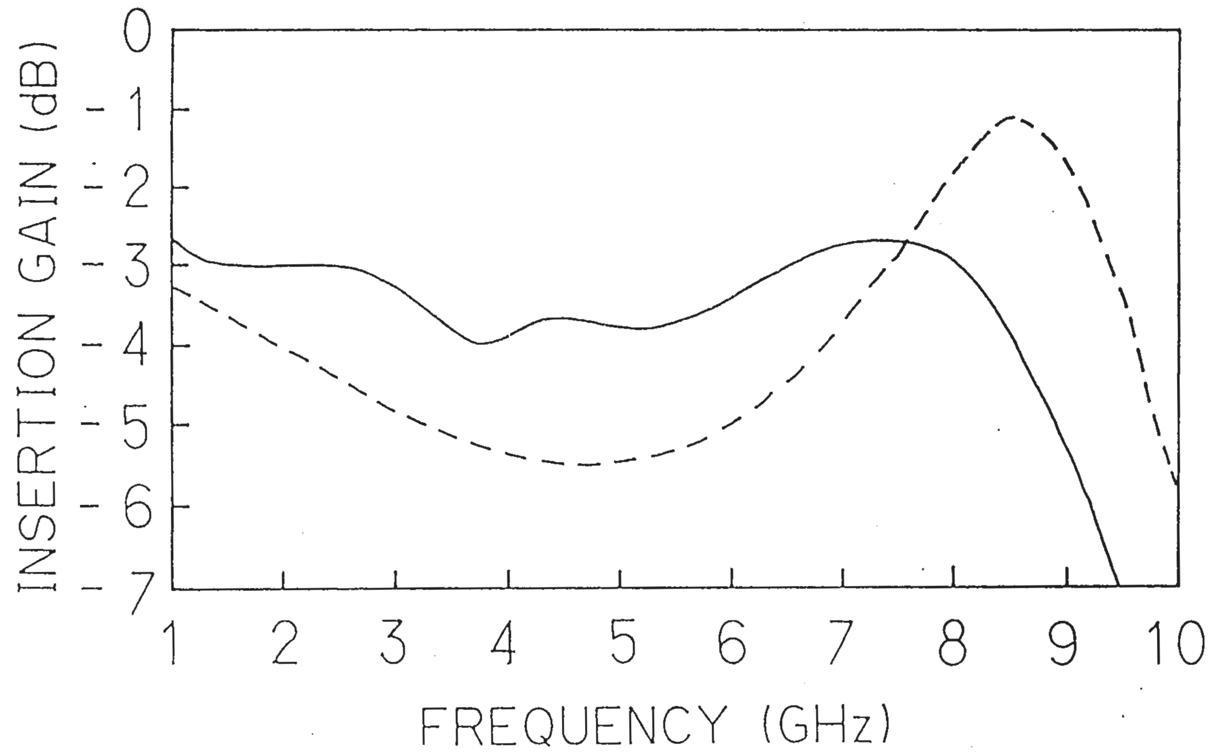
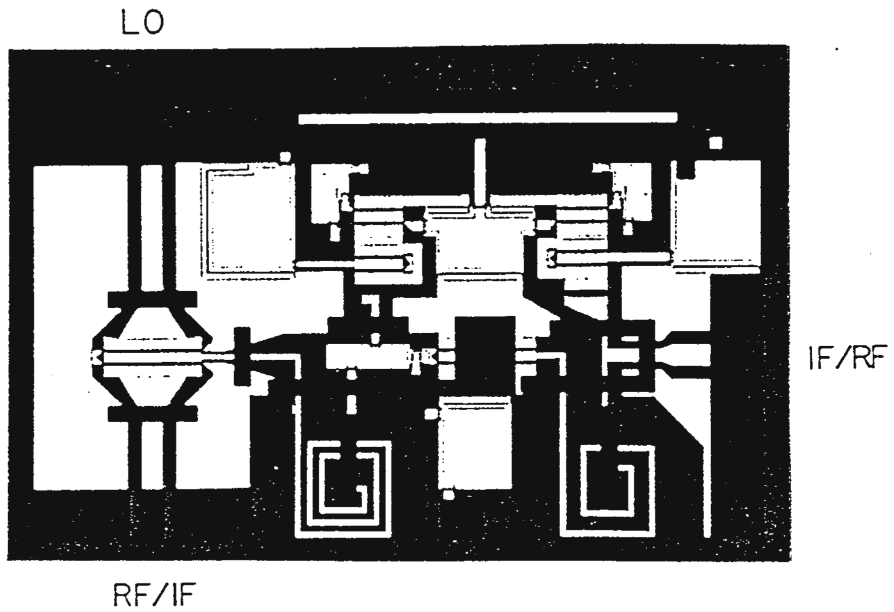
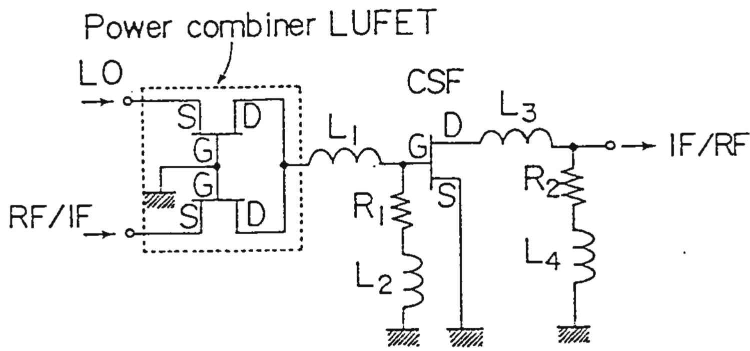


Fig. 2.25 Insertion loss vs. frequency characteristics of an isolator composed of one six-port cell and an LR circuit. Solid: measured (with feedback loop), dash: calculated (without feedback loop).



(a)



(b)

Fig. 2.26 . Photograph and equivalent circuit diagram of a mixer MMIC using an in-phase combiner LUFET. The size is 0.9mm×1.4mm. (a) Photograph. (b) Equivalent circuit diagram.

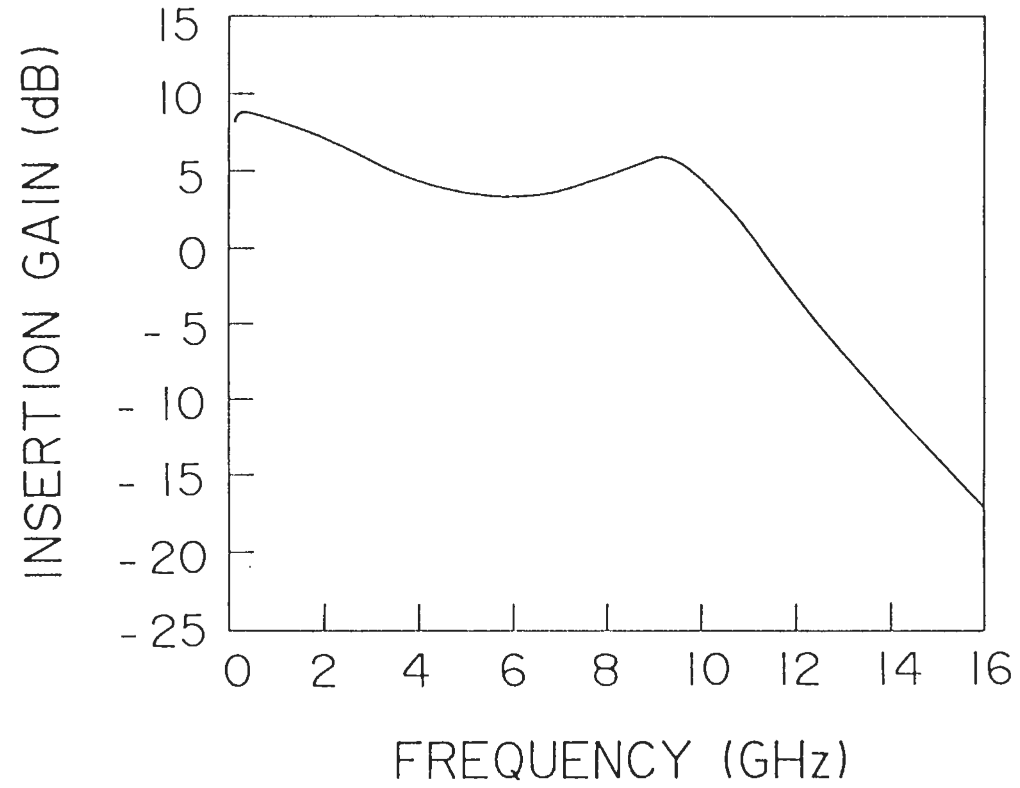


Fig. 2.27 Insertion gain vs. frequency characteristic of the mixer MMIC in linear operation.

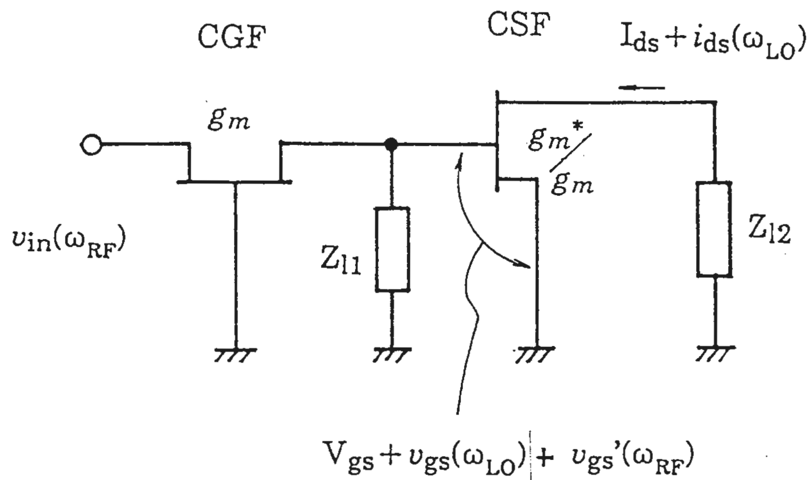


Fig. 2.28. A simplified equivalent circuit diagram for the calculation of the mixer conversion gain $G_M(\omega)$.

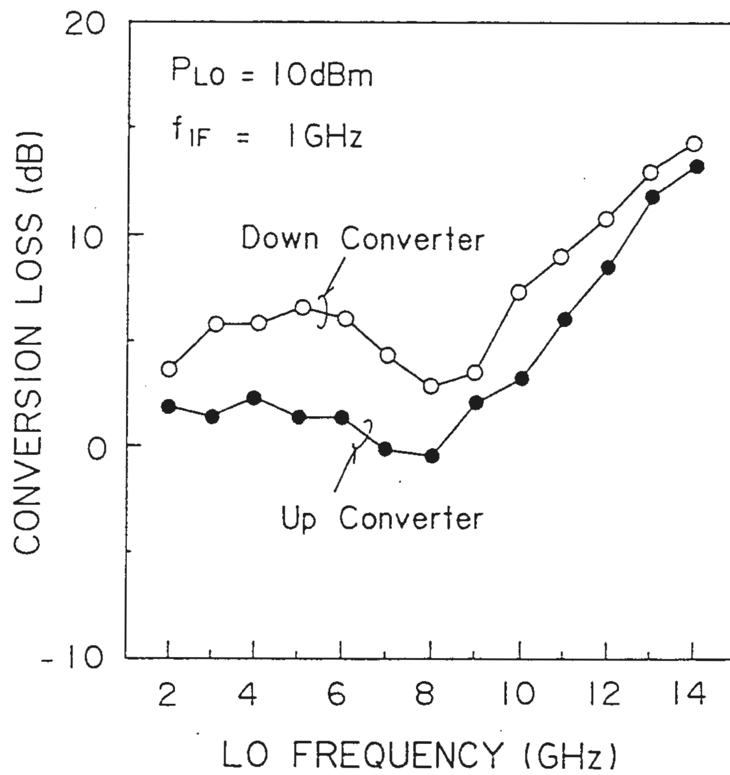


Fig. 2.29 Measured conversion loss when the mixer MMIC is used as a down- and up converter, where the IF is 1GHz and the local power P_{LO} is 10dBm.

Fig. 2.30 Configuration of a balanced mixer LUFET which is formed by an in-phase divider, in-phase combiner LUFETs and a slotline T junction as out-of-phase divider.

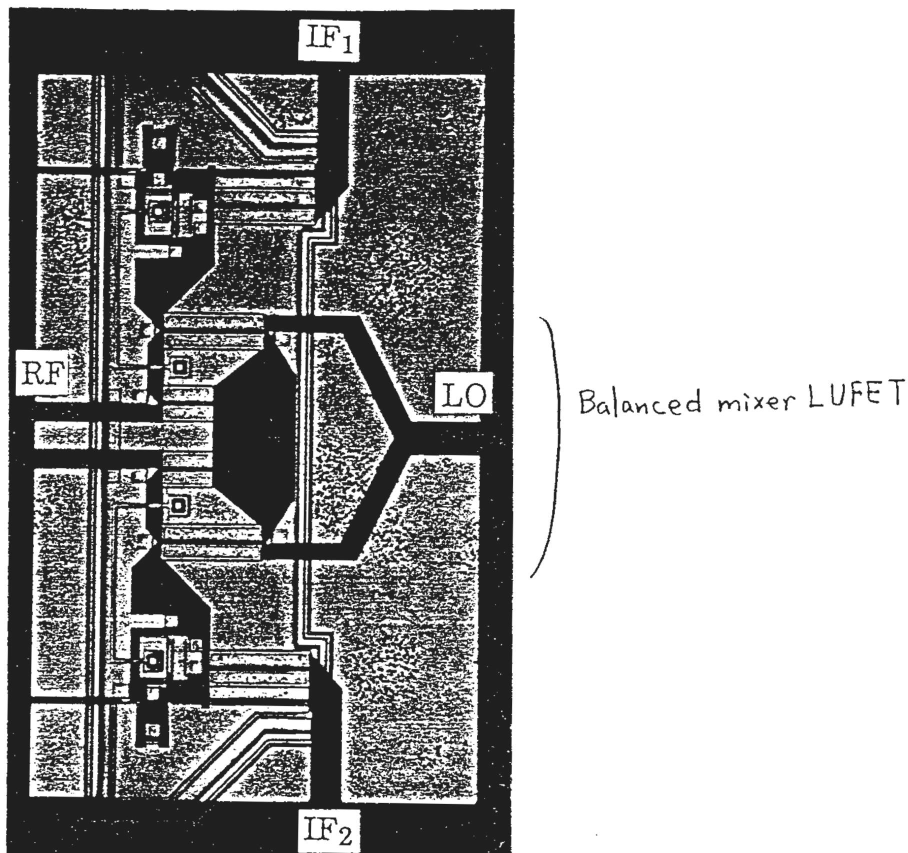


Fig. 2.31. Photograph of a balanced mixer MMIC. The chip size is 0.7mm×1.1mm. The area of the LUFET is about 0.3mm^2.

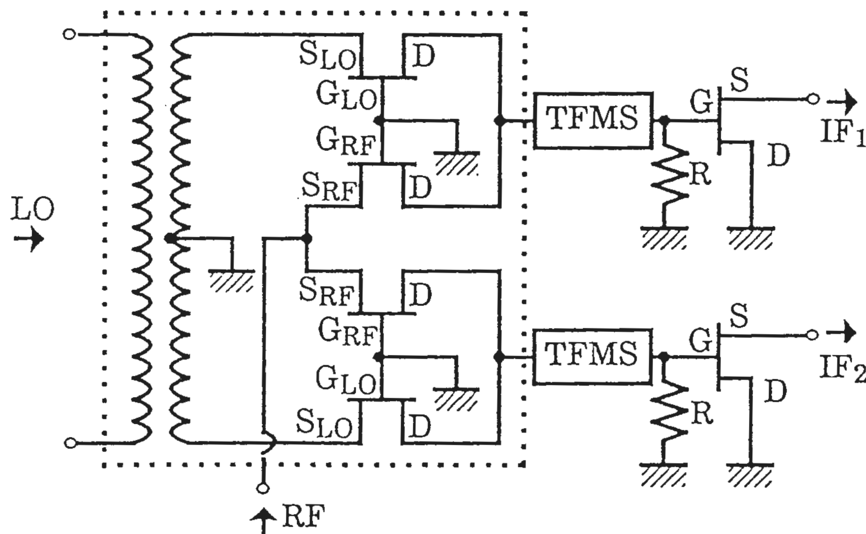


Fig. 2.32 Equivalent circuit diagram of the balanced mixer MMIC, where the area enclosed by the dashed line is the balanced mixer LUFET.

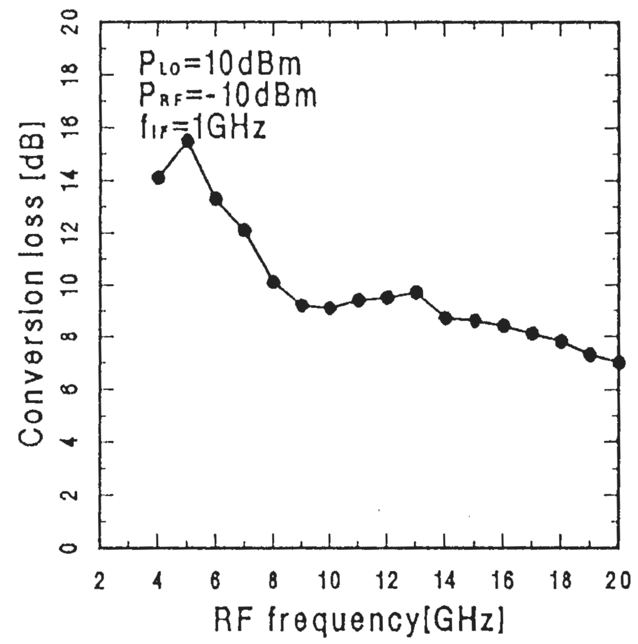
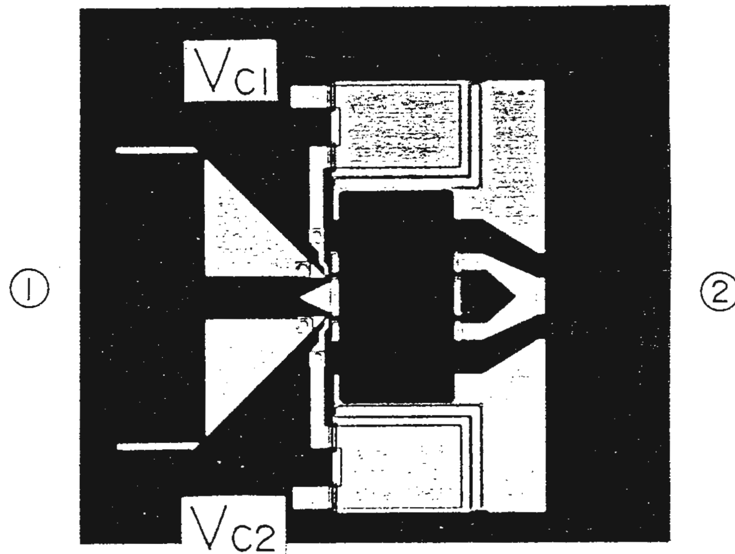


Fig. 2.33 Measured conversion loss vs. frequency characteristic of the balanced mixer MMIC.



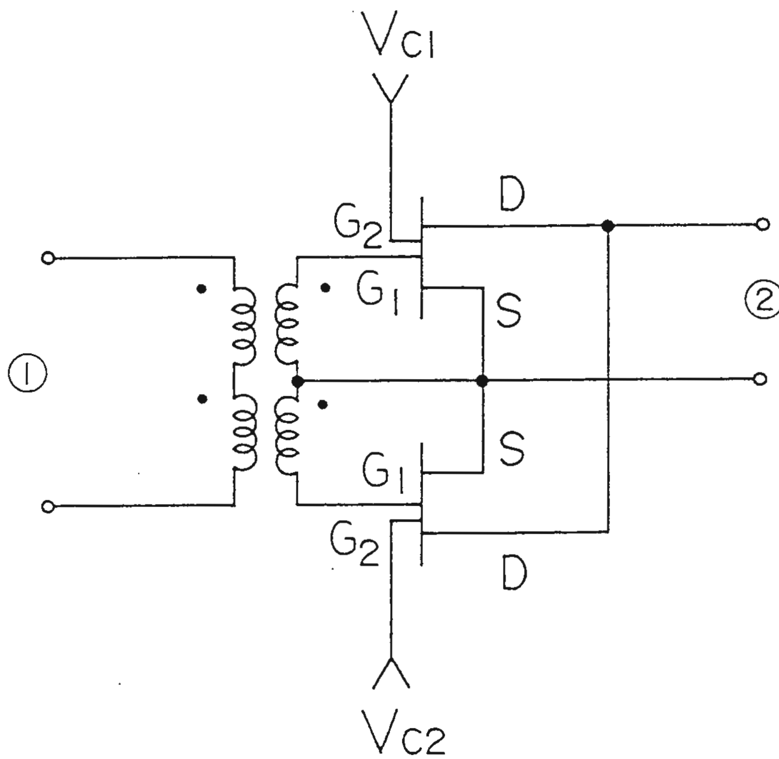


Fig. 2.34 . Photograph and equivalent circuit diagram of a balanced modulator LUFET which is implemented using a dual-gate phase inverter LUFET. The chip size is 0.6mm × 0.5mm.

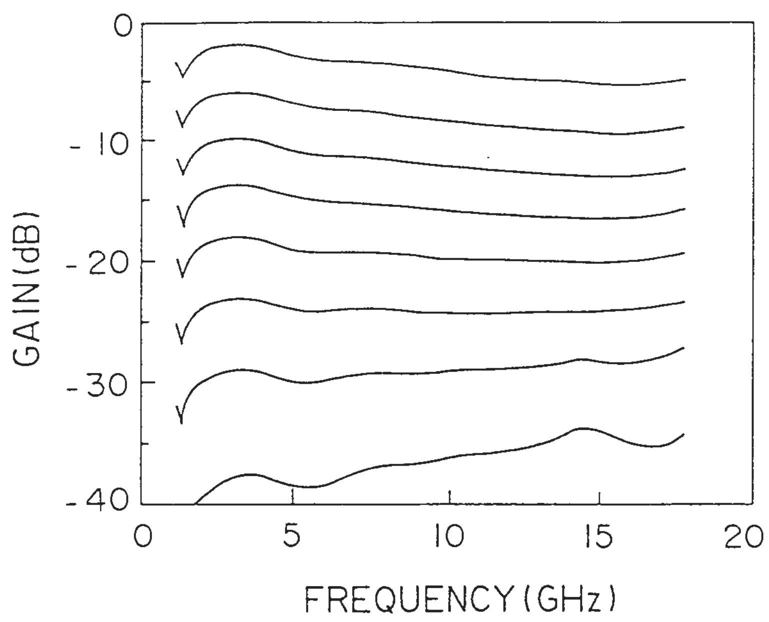


Fig. 2.35. Measured variable gain characteristics of the balanced modulator.

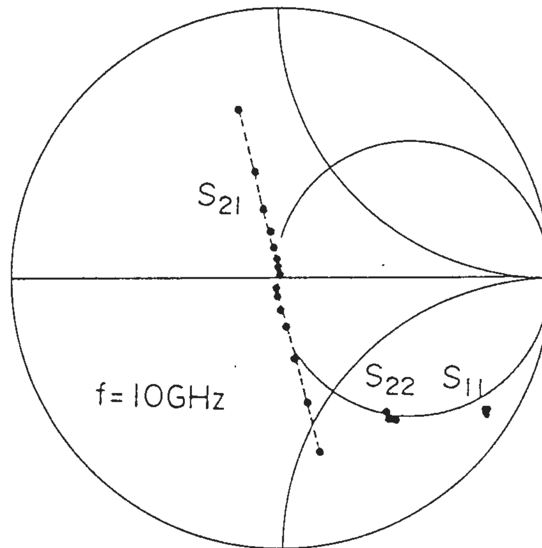
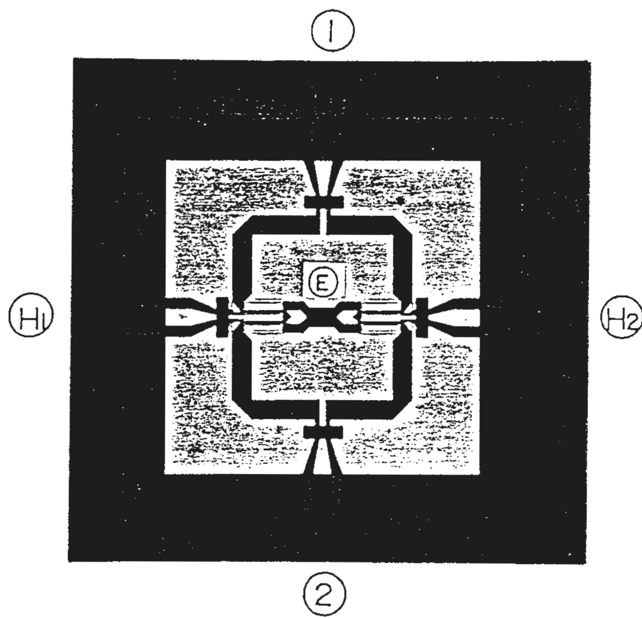


Fig. 2.36. Gain and impedance change by the second gate bias voltage. The measurement frequency is 10GHz.



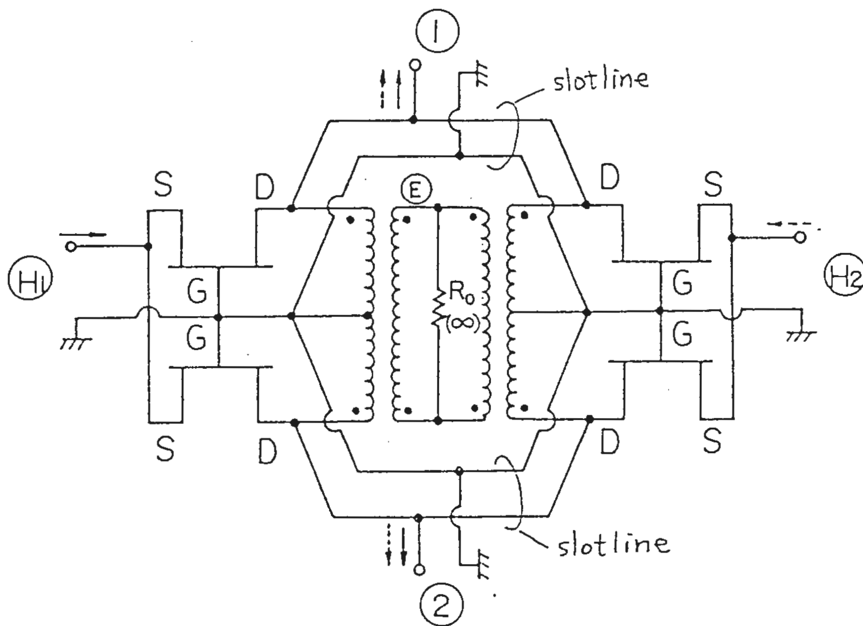


Fig. 2.37. Photograph and equivalent circuit diagram of a signal path switch utilizing a magic T LUFET, where two magic T LUFETs are symmetrically combined. The chip size is 1mm×1mm, while the intrinsic area is less than $0.5mm^2$.

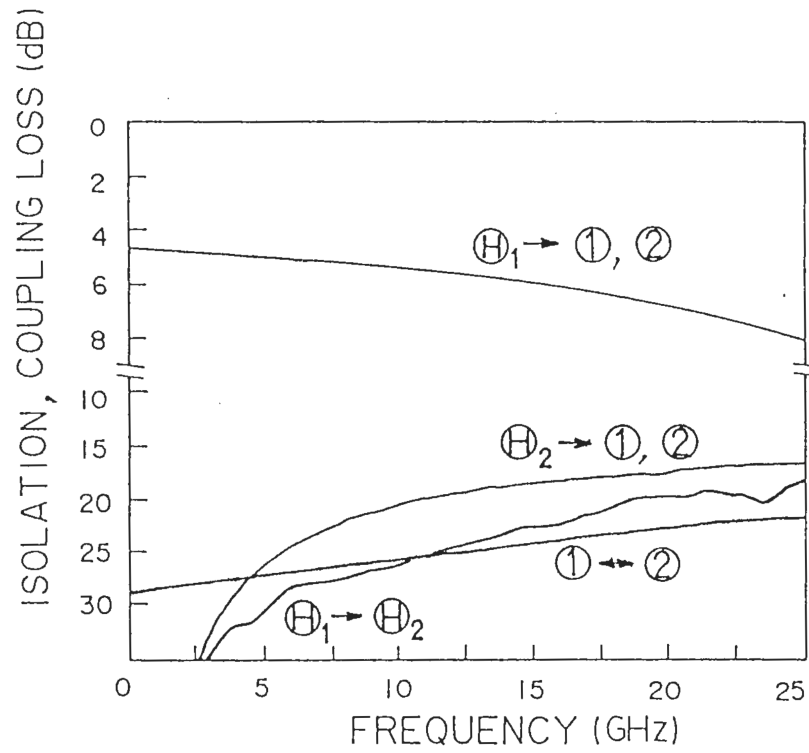


Fig. 2.38. Measured coupling loss and isolation characteristics of a signal path switch MMIC.

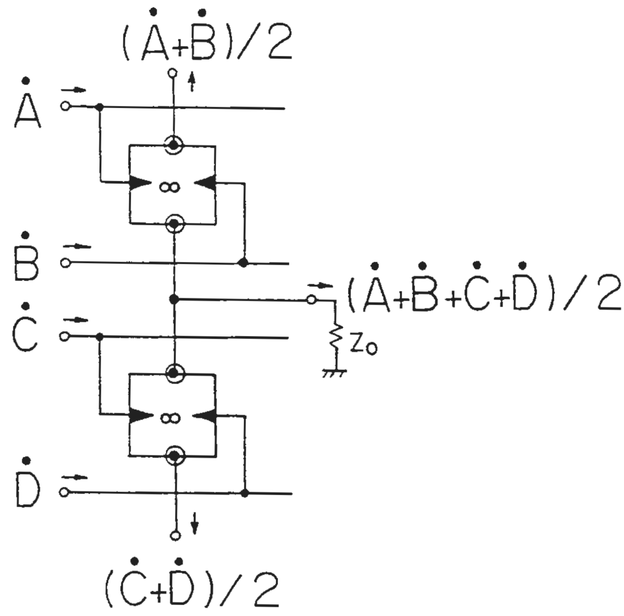


Fig. 2.39 4-Port Signal Combiner Using Two Divider/Combiner Modules.

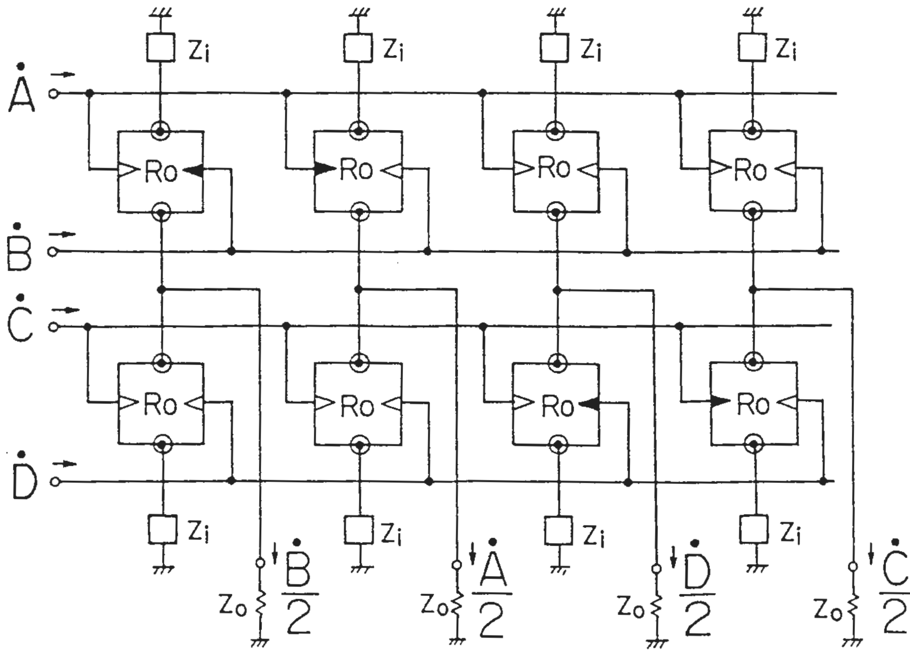


Fig. 2.40 4 x 4 Switch Matrix Using 8 Divider/Combiner Modules.

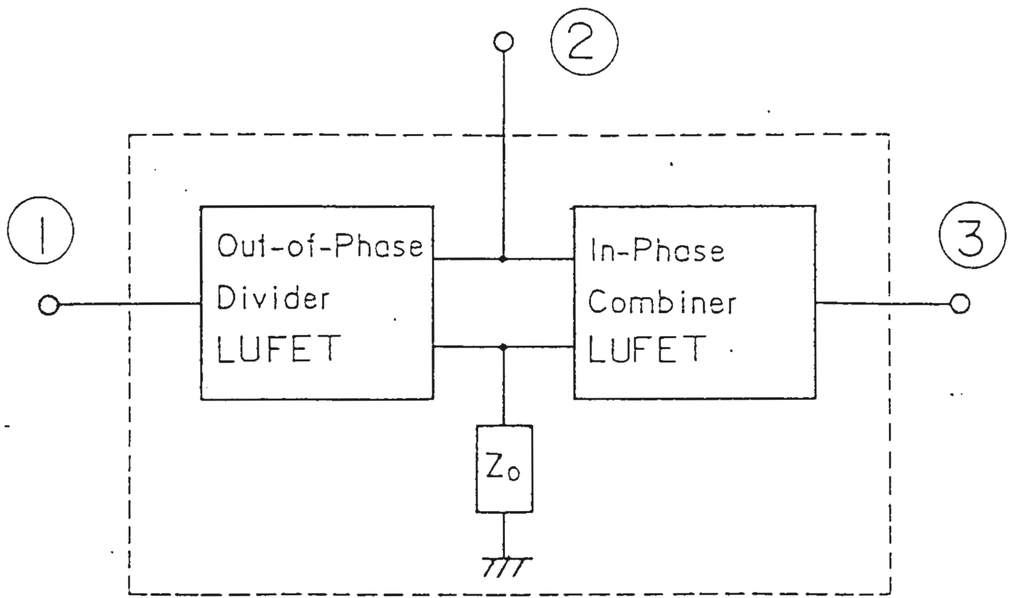


Fig. 2.41. A basic quasi-circulator configuration composed of an out-of-phase divider LUFET and an in-phase combiner LUFET.

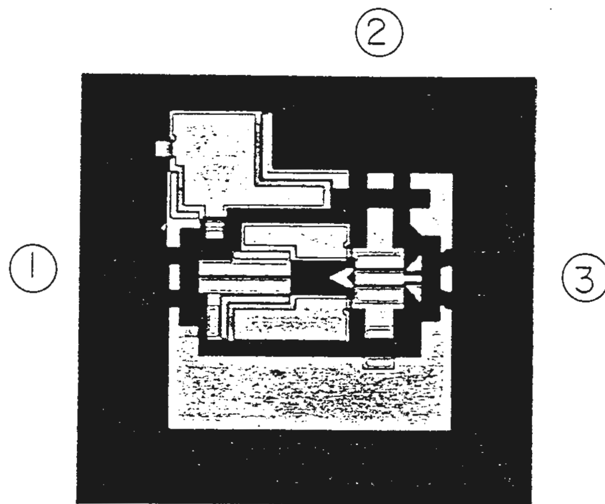


Fig. 2.42. Photograph of a quasi-circulator MMIC. The chip size is 0.6mm×0.5mm.

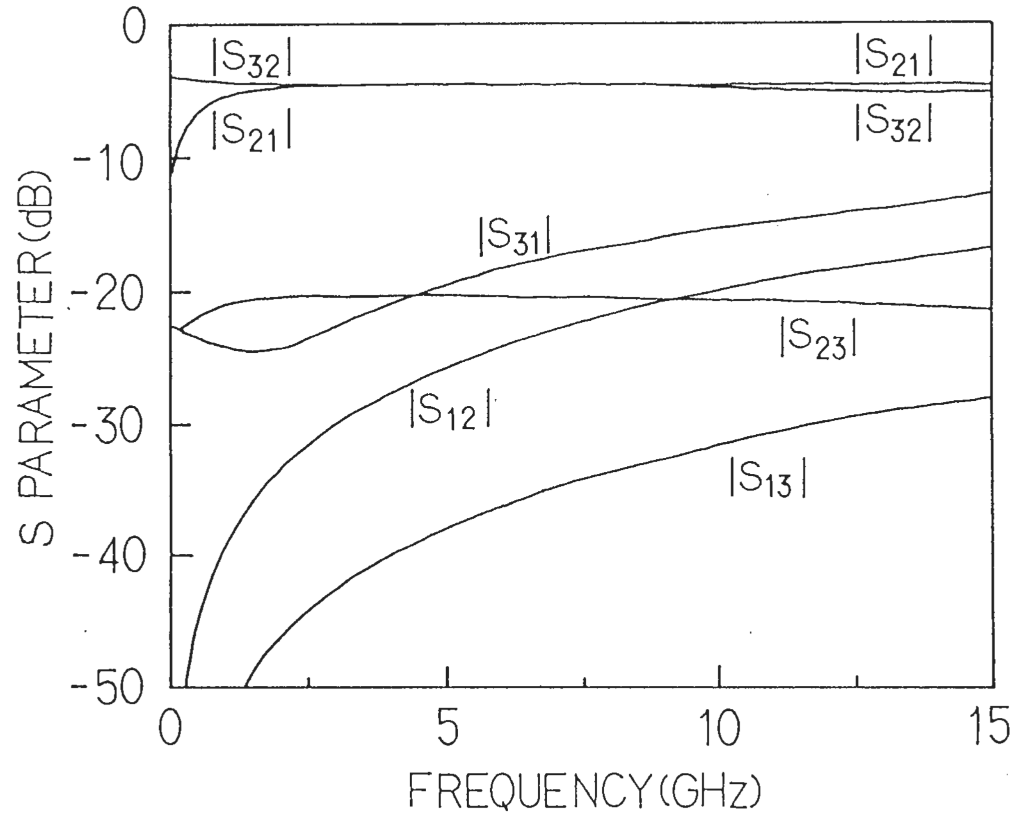


Fig. 2.43 . Measured performance of the quasi-circulator.

2.5. 考察
2.5. Discussion

Combiner and divider Line-Unified-FETs (LUFETs) have been proposed and demonstrated. Some effective modifications such as extended combiner LUFETs, magic T LUFETs, and phase inverter LUFETs are also demonstrated with their simple configurations. The basic and modified LUFETs are, by themselves, circuit-function modules and have very small chip sizes approaching 1/5 that of conventional MMICs. The combiner and divider LUFETs are, in a sense, active T junctions realized in a very small size nearly equal to that of conventional FETs. MMICs at various levels of integration can be implemented on a reasonably small chip by modifying and combining the LUFETs. Furthermore, MMICs employing LUFETs offer multioctave-band operation due to the absence of frequency dependent distributed lines, and also allow active matching and easy grounding.

Furthermore, wideband performance of mixers, combiner/dividers, magic Ts, modulators, switches and circulators using the LUFETs, as well as their simple configurations and very small chip sizes of approximately $0.5mm^2$, has been demonstrated. The size is less than 1/2 that of conventional MMICs. LUFETs used as fundamental circuit-function modules allow designing reasonably small, multifunction MMICs with little concern for MMIC chip size. The design efficiency can also be enhanced when a systemized LUFET library is prepared. Combination of the LUFETs and thin film microstrip (TFMS) lines should further enhance function integration on a chip. These features of the LUFET should prove valuable in realizing miniaturized, generic-use MMICs, antenna control MMICs, and RF signal processing MMICs.

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付録　周波数変換器の周波数特性解析
APPENDIX

Mixer conversion gain G_M formulated by eq. (2) is derived from the simplified equivalent circuit diagram shown in Fig. 7. The dc drain current I_{ds} of the CSF in the saturated current region is represented by (A1).

$$I_{ds} = I_{dss}(1 - V_{gs}/V_p)^2 (1 + V_{ds}/R_{do}I_{dss}), \qquad \text{when } V_{gs} > V_p$$

$$I_{ds} = 0, \qquad \text{when } V_{gs} < V_p \tag{A1}$$

where, V_{gs} and V_{ds} are dc gate- and drain bias, respectively, and R_{d0} is the output conductance. When $v_{gs}(\omega_{LO})$ is the local signal voltage across the CSF gate and source, (A1) is rewritten as (A2).

$$I_{ds}+i_{ds}(\omega_{LO})=I_{dss}\,[1-(V_{gs}+v_{gs}(\omega_{LO}))/V_p]^2\,[1+K(V_{ds}+v_{ds}(\omega_{LO}))],$$

$$\text{when } V_{gs}+v_{gs}(\omega_{LO})>V_p \qquad \text{(A2)}$$

$$I_{ds}+i_{ds}(\omega_{LO})=0, \qquad \text{when } V_{gs}+v_{gs}(\omega_{LO})<V_p$$

where, $i_{ds}(\omega_{LO})$ and $v_{ds}(\omega_{LO})$ are the ac drain current voltage due to the $v_{gs}(\omega_{LO})$. K is a constant equal to $(R_{do}I_{dss})^{-1}$.

The nonlinear transconductance $di_{ds}(\omega_{LO})/dv_{LO}(\omega_{LO})$ due to gate-source nonlinearity is derived from (A2) as follows, when $V_{gs}+v_{LO}(\omega_{LO})>V_p$:

$$di_{ds}(\omega_{LO})/dv_{gs}(\omega_{LO})$$

$$=-(2I_{dss}/V_p)\,[(1-V_{gs}/V_p)-v_{gs}(\omega_{LO})/V_p]\,[1+K(V_{ds}+v_{ds}(\omega_{LO}))]$$

$$+I_{dss}\,[(1-V_{gs}/V_p)-v_{gs}(\omega_{LO})/V_p]2\,K\,dv_{ds}(\omega_{LO})/dv_{gs}(\omega_{LO}), \qquad \text{(A3)}$$

while the transconductance is zero when $V_{gs}+v_{gs}(\omega_{LO})<V_p$. Using a relation that $v_{ds}(\omega_{LO})=-g_m{}^*Z_{12}v_{gs}(\omega_{LO})$, (A3) can be rewritten as (A4) which is a polynomial function of $v_{gs}(\omega_{LO})$.

$$di_{ds}(\omega_{LO})/dv_{gs}(\omega_{LO})$$

$$=-I_{dss}\,[2(1+KV_{ds})/V_p+Kg_m{}^*Z_{12}(1-V_{gs}/V_p)]\,(1-V_{gs}/V_p)$$

$$+2I_{dss}\,(1+KV_{ds})\,v_{gs}(\omega_{LO})/V_p{}^2$$

$$-3I_{dss}Kg_m{}^*Z_{12}v_{gs}{}^2(\omega_{LO})/V_p{}^2 \qquad \text{(A4)}$$

where, $g_m{}^*Z_{12}$ represents the ac voltage gain of CSF at each $v_{gs}(\omega_{LO})$. The second term does not include any $g_m{}^*$ and Z_{12}.

The second term in (A4) provides IF current in load Z_{12} when RF signal $v_{gs}'(\omega_{RF})$ is applied to the CSF gate due to $v_{in}(\omega_{RF})$ at the CGF input port, where $v_{gs}'(\omega_{RF}) = g_m Z_{11} v_{in}(\omega_{RF})$. Rewriting $v_{gs}(\omega_{LO})$ and $v_{in}(\omega_{RF})$ as follows:

$$v_{gs}(\omega_{LO}) = |V_{LO}| \cos \omega_{LO} t$$

$$v_{in}(\omega_{RF}) = |V_{RF}| \cos \omega_{RF} t, \tag{A5}$$

the IF output voltage $v_{IF} = |V_{IF}| \cos(\omega_{RF} - \omega_{LO})t$ across load Z_{12} is given by (A6).

$$|V_{IF}| = [g_m Z_{11} Z_{12} I_{dss}(1 + KV_{ds})/2V_p^2]\, |V_{LO}|\, |V_{RF}| \tag{A6}$$

where, Vgs is settled at Vp for an effective mixer operation. Therefore, the voltage conversion gain $G_M(\omega)$ is as follows:

$$G_M(\omega) = |V_{IF}| \,/\, |V_{RF}| = [g_m Z_{11} Z_{12} I_{dss}(1 + KV_{ds}) \,/\, 2V_p^2]\, |V_{LO}| \tag{A7}$$

On the other hand, the voltage gain $G_C(\omega)$ when the CSF is in a linear state is given by (A8).

$$G_C(\omega) = g_m{}^2 Z_{11} Z_{12} \tag{A8}$$

Comparing (A7) and (A8), we obtain eq.(2).

$$G_M(\omega) = G_C(\omega)\, [I_{dss}(1 + KV_{ds}) \,/\, 2g_m V_p^2]\, |V_{LO}| \tag{A9}$$

where, K = 0 in eq. (2).

3. 多層化MMIC
3. Multilayer MMIC

Conventional microwave and millimeter-wave passive MMICs constructed with quarter-wavelength transmission lines occupy large areas on MMIC chips, because semi-insulating GaAs wafers, hundreds of µms thick, are used for the substrates of the transmission lines, which are usually microstrip lines. Although coplanar waveguides (CPWs) often used in uni-planar MMICs do not depend on wafer thickness, the degree of size reduction is limited due to the center conductor and grounds on the same surface of the substrate [3.1].

To overcome the problem of size reduction, and also to enhance circuit design flexibilities, we propose a 3µm×3-layer dielectric film structure, and use of the film for the substrate of microwave and millimeter-wave transmission lines. 90-degree and 180-degree hybrids, Wilkinson dividers, and distributed amplifiers are implemented in a very small area, less than $1mm^2$, by using the valuable features of miniature, thin film transmission lines [3.2-3.4]. This innovation and the LUFET mentioned in Chapter 2 are extremely effective for integrating various circuit functions in a reasonably small MMIC chip because of the very small size, high design flexibilities, and easy transition between them.

3.1. 多層化MMIC伝送線路とその特徴
3.1. Thin Film Transmission Lines and the Features

Various kind of miniature transmission lines can be realized using a thin film structure on a surface of semi-insulating substrate. Typical examples of thin film transmission lines are shown in Fig. 3.1. Each transmission line is formed on one side of a GaAs wafer, and offers a significantly reduced line width due to the thin, several-µm thick dielectric film, which is deposited or coated over the base metal on the GaAs wafer surface. The electric field is concentrated between the metal

strip and the ground. Fig. 3.1 (a) is a thin film microstrip (TFMS) line [3.5], (b) inverted TFMS line, and (c) and (d) quasi-CPWs. The 50Ω line width of these lines is between 5μm and 20μm, and less than twice the film thickness. The width is similar to that of high impedance microstrip lines often used in the recent, generic-use compact MMICs, and also less than 1/10 that of 50Ω microstrip lines on a GaAs wafer.

Silicon oxynitride (SiON,$\varepsilon_r = 5.0$) and polyimide (SP-510, $\varepsilon_r = 3.3$) are used for the dielectric film. SiON is deposited in 3μm-thick layers, using a low-temperature plasma-CVD process. Polyimide is coated in 2.5μm-thick layers using a spin-coating method to obtain layers well-controlled in thickness [3.4]. These films have much lower film stress compared with other insulators such as SiO_2 and Si_3N_4 on GaAs substrates, and allow fabricating 10μm-thick dielectric films. Furthermore, polyimide flattens the surface of each layer.

The TFMS line, as well as the other thin film transmission lines in Fig. 3.1, offers the following features:

① a meander-like configuration with a spacing only 2 or 3 times that of the film thickness, which effectively miniaturizes quarter-wavelength transmission lines;

② a high isolation crossover composed of narrow-width lines on two different layers, which enhances layout flexibilities, maintains high frequency operation, and achieves chip size reduction;

③ a vertical connection between circuit elements on the dielectric layers and GaAs substrate, which eliminates lines and crossovers degrading high frequency operation and performance.

Fig. 3.2 shows a photograph of a meander-like TFMS line. The meander-like configuration widely used in the multilayer MMICs mentioned below, allows close agreement between measured and calculated performance due to negligibly small parasitics between lines and at corners [3.3]. Figure 3.3 shows a photograph of a TFMS line crossover. The lower metal strip has pads on both

sides and the upper metal strips are continuously fabricated. The metal strips in the direction A-B are connected via through holes on both sides of the lower metal strip. Fig. 3.4 shows the measured characteristics of a 50Ω TFMS line crossover. Isolation is better than 30dB and return loss is better than 20dB up to 25GHz. Fig. 3.5 shows vertical connections through dielectric layers. Sharp holes are formed through each SiON layer by using dry etching, and cone-shaped holes are formed through the polyimide film by using chemical etching.

3.2. 損失特性
3.2. Loss Characteristics

Thin film transmission lines, like conventional high-impedance microstrip lines, are not lossless, but rather lossy transmission lines, where the conductive loss is dominant. The surface resistivity R_s of the metal and the transmission loss *Loss* of the TFMS line, as a function of frequency f, are given by the following equations [3.5]:

$$R_s(f) = R_{s0} \times tK\sqrt{f} / (1-e^{-tK\sqrt{f}}) \quad (\Omega/\square) \qquad (3.1)$$

$$Loss \simeq 8.68 R_s(f)[1/Z_0 \cdot H/W][L/H] \quad \text{(dB/m)} \qquad (3.2)$$

where R_{s0} is the surface resistivity for dc current, t is the metal thickness, and Z_0, L, and W are line impedance, length, and strip width. H is the dielectic film thickness. K is a material constant giving the skin depth; $\delta = (K\sqrt{f})^{-1}$. Because $[1/Z_0 \cdot H/W]$ is nearly constant, larger H and smaller R_{s0} are required for lower loss. However, thickness H of around 10μm is effective for achieving both drastic chip-size reduction and reasonably low transmission loss. R_{s0} depends on the strip metal and its fabrication process.

Equation (3.1), which gives the R_s a finite value at zero frequency, is derived based on a fact that the strip metal thickness is smaller than the skin depth. The total current I which flows through the cross section of the TFMS line is given by eq. (3.3).

$$I = I_0 \int_0^t e^{-x/\delta} dx = I_0 \delta (1 - e^{-t/\delta}) \qquad (3.3)$$

where, I_0 is the current density on the surface of the metal, t is the thickness of the metal, δ is the skin depth represented as $\delta = 1/\sqrt{\pi \mu_0 \sigma f}$, where μ_0 and σ are the magnetic permeability of free space and the conductivity of the metal, respectively. We define the skin depth of the TFMS, δ', as shown in equation (3.4), because $I = I_0 \delta$ when t is sufficiently large compared to δ.

$$\delta = \delta'(1 - exp[-\frac{t}{\delta}])\qquad(3.4)$$

From this definition, surface resistivity $R_S(f)$ of the TFMS line is obtained as follows:

$$R_s(f) = \frac{\rho}{\delta'} = \frac{\sqrt{\pi\mu_0\sigma f}}{1 - e^{-t/\delta}}\qquad(3.5)$$

where, ρ is the resistivity of the metal which is reciprocally equal to σ. By using the surface resistivity for dc current, R_{S0}, equation (3.5) can be written as equation (3.1). Fig. 3.6 shows measured and calculated loss characteristic of a TFMS line with 5μm line width, 1.5mm line length, and 3μm dielectric film thickness. Both characteristics closely agree, where measured R_{S0} value of 0.029 (Ω/□), t=1μm, and $\rho = 2.4 \times 10^{-6} \Omega \cdot cm$ are used in the calculation. Fig. 3.7 compares the loss characteristics of the TFMS line and conventional microstrip line on a GaAs substrate. The loss characteristics of the TFMS lines with different metal thicknesses are shown in the figure. The film thickness around 10μm offers a transmission loss comparable to that of the 50Ω microstrip line on a GaAs substrate, when $t=H/3$. Metal thickness t of $H/3$ is the maximum value when other thin films are stacked onto the TFMS line for multilayer MMICs. In the actual multilayer MMIC implementations, metal thickness of 1μm is used for flatter film surface and relatively low R_S. We determined to increase the film thickness and widen the line width to obtain lower loss, thin film transmission lines. Fig. 3.8 shows the estimated area of the TFMS lines and microstrip lines as a function of film thickness H. In this estimation, the "area" is defined as the product of 3 line widths times a quarter-wavelength, where each transmission line width is determined by the point at which line impedance is 50Ω. The SiON film dielectric constant is 5.0, and that of GaAs is 12.9. The area of TFMS lines on a 6-to-10μm-thick SiON, for example, is about 1/10 tht of conventional microstrip lines on a 150μm-thick GaAs substrate.

3.3. 多層誘電体膜構造を用いた超小型MMIC
3.3. Multilayer MMIC Using a 3μm×3-Layer Structure

Examples of multilayer MMICs using the advantages mentioned in section 3.1 are demonstrated in Figures 3.9-3.18. Although the examples are implemented using only TFMS line, these TFMS lines can be easily replaced with the other thin film transmission lines. Combinations of different lines also realize more efficient circuits, which is one of our further programs.

Following MMICs are implemented by using SiON and polyimide, where a dc surface resistivity R_{s0} of 0.029Ω/□ was used in the performance predictions according to an advance test data. Measured R_{s0} of the fabricated strip metal on the materials are 0.06Ω/□ and 0.03Ω/□, respectively.

3.3.1. マジック T
3.3.1.Magic T

A very small, wideband magic T MMIC is shown in Fig. 3.9 [3.5]. The chip size is 0.9mm×1.0mm and the intrinsic area is only 0.3mm×0.5mm. The chip area about 1/10 the size of a conventional magic T is achieved. This magic T is composed of a slotline series T junction, a microstrip parallel T junction, and two quarter-wavelength, 70Ω TFMS lines, which combine the series and parallel T junctions. The TFMS lines are fabricated using a 3μm-thick SiON film deposited on the slotline T junction. Ports Ⓔ and Ⓗ correspond to the E- and H-arms of a metallic waveguide magic T, respectively, and ports ① and ② are the remaining two ports . This magic T using a dielectric film as thin as 3μm requires the 70Ω TFMS line width of as narrow as 2μm, which has two times greater value of R_{s0} than required for 5dB coupling loss (see reference [3.5] for more detail informations). A 50Ω TFMS line with 5μm line width is effectively used in the actual design. The measured performance of the fabricated thin film magic T is

shown in Fig. 3.10. The following performance is obtained in the frequency range from 4GHz to 18GHz: coupling losses between ports Ⓔ and ①, ② and between Ⓗ and ①, ② is better than 5dB; isolation between ports Ⓔ and Ⓗ and between prts ① and ② is better than 30dB and 12dB, respectively. The return loss at each port is better than 10dB in the same frequency range.

This magic T is the first succesful multilayer MMIC using a thin film and demonstrates a meander-like TFMS line configuration along with an easy transition between TFMS lines and coplanar lines. Novel multilayer structurs which provides further advantages to the multilayer MMIC are described below.

3.3.2. 90度ハイブリッド(ブランチライン回路)
3.3.2. 90-degree hybrid (Branch-line Coupler)

A 15GHz 90-degree hybrid (branchline coupler) MMIC is shown in Fig. 3.11 [3.2,3.4,3.6]. The 35Ω TFMS lines between ports ①, ② and between ports ③, ④ are formed on a 5μm-thick polyimide layer coated over the ground on the surface of a GaAs wafer. The line width is 18μm. Another 2.5μm-thick polyimide layer is coated after the 35Ω metal strip is applied to the 5μm-thick polyimide layer. 50Ω TFMS lines between ports ①, ④ and between ports ②, ③ are formed on the top surface of the 7.5μm-thick film. The line width is 16μm. Each metal strip level is connected to the other metal strip level via through holes at the corresponding ports. The 35 and 50Ω TFMS lines on the different layers have almost the same line width and insertion loss. Therefore, the frequency characteristics are balanced.

The chip size is 1.3mm×1.6mm, while the intrinsic area after subtracting the input and output lines is only 0.7mm×1.0mm. Fig. 3.12 shows the measured and calculated performance. Both performances agree closely. This branchline coupler exhibits a coupling loss of 5.5dB±0.5dB, isolation better than 15dB (24dB

at the center frequency), and return loss better than 10dB at frequencies between 12GHz and 16GHz.

3.3.3. 180度ハイブリッド(ラットレース回路)
3.3.3. 180-degree hybrid (Rat-Race Hybrid)

A 20GHz 180-degree hybrid (rat-race hybrid) using 3μm×3-layer SiON film is shown in Fig. 3.13, where a TFMS line crossover is employed [3.3,3.4,3.7]. The crossover in the rat-race hybrid MMIC allows the isolation ports ① and ④, which are diagonally allocated in the conventional rat-race hybrids, to be allocated on the other side of the hybrid from the input ports ② and ③. Each 70Ω strip width is 7μm. Measured isolation between the upper and lower strips is greater than 35dB up to 25GHz, due to stray capacitance as small as 0.001pF between the strips. The chip size is 1mm×1mm, and the intrinsic area is less than 0.7mm×0.7mm. This rat-race hybrid exhibits, as shown in Fig. 3.14, coupling loss of 6dB±1dB, isolation better than 20dB (30dB near the center frequency), and return loss better than 20dB between 17GHz and 23GHz.

3.3.4. 分布型増幅器
3.3.4. Distributed Amplifier

The 6-stage distributed amplifier MMICs shown in Fig. 3.15 offer another application of the meander-like configuration and crossover of the TFMS lines [3.2,3.8]. The MMICs are implemented using SiON film, and the chip size is 0.8mm×1.3mm. The two MMICs are designed using the same equivalent circuit scheme and parameters to achieve a 5dB gain across 0.5GHz and 18GHz. This sophisticated layout (b) is difficult in conventional planar MMICs. The layout

flexibility allows enhancing circuit-packing density and heat radiation. In addition, TFMS lines fabricated over the RF bypath capacitors contribute to the chip size reduction. Fig. 3.16 shows the measured and calculated performance of both distributed amplifier MMICs.

3.3.5. ウィルキンソンディバイダ
3.3.5. Wilkinson Divider

A 12GHz 4-port Wilkinson divider MMIC with a chip size of 1.2mm×1.0mm is shown in Fig. 11 [3.2, 3.3, 3.9]. Four resistors and an H-shaped conductor connecting the resistors are clustered on the surface of a GaAs wafer. Input and output CPWs are, in this case, also formed on the same surface. A metal, which connects ground conductors of the CPWs via through holes, is applied on the first 3μm-thick SiON film. Four quarter-wavelength, TFMS line transformers are formed on a second 6μm-thick SiON film. Finally, the above resistors for output isolation and the TFMS transformers are connected vertually via through holes. A high isolation among the output ports, better than 30dB, is obtained at the center frequency, due to the absence of undesirable lines and crossovers for connecting the resistors and transformers; in other words, an electrically symmetrical configuration. Measured isolation characteristic is shown in Fig. 3.18 along with the power dividing characteristic.

3.4. 考察
3.4. Discussion

The "multilayer MMIC" mentioned in this chapter provides excellent advantages for miniaturizing microwave passive circuits in monolithic form. A magic T, hybrids, and multiport Wilkinson dividers, which are conventionally difficult to be implemented in MMIC chip due to the frequency -dependently large size, have been fabricated in a very small area, less than 1mm^2. The features of a multilayer thin dielectric film structure; such as meander-like configurations, line crossovers, and vertical connections, have been fully employed resulting in an enhancement of design-flexibilities. However, further progress in this technology is expected because the examples above is just at the start point. The multilayer and LUFET MMIC concepts should prove valuable in realizing reasonably small, multifunction MMIC chips, and the combination of the LUFET and thin film transmission lines should further enhance function integration on a chip. What to be done in the next generation is to design and verify 1-chip, multifunction MMICs by using the both concepts, and to widely expand MMIC's abilities.

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4. おわりに
4. Conclusion

本報告は、ATRで新しく提案した「線路一体化FET」および「多層化MMIC」の概念、および、背景あるいは動機付けとなる研究のねらいを理解して頂くために作成した。このため、詳細なデータやその他多くの試作回路を省略した。詳細については参考文献、他のテクニカルレポート、測定データ集、等を参照して頂きたい。また、アクティブインダクタについては、原研究員のテクニカルレポート[1.57]で詳述しているので、本報告では省略した。

これまでの3年間の研究により、種々の機能回路を従来に比べて大幅に小型化する基本技術をおおむね明らかにすることができた。各章ごとに示した外部の研究·開発状況で分かるように、MMIC小型化に向けたアプローチの仕方は様々である。一方、1チップ上に多くのマイクロ波回路を集積する"Multi-function MMIC"の研究·開発が最近活性化しつつある。「小型化」および「集積化」は互いに相補う技術であり、一方をおろそかにして他方を成し遂げることはできない。ATRのMMIC技術は「小型化」を大幅に前進させたが、「集積化」についての検討は現時点で不十分である。今後は、将来の移動無線通信システムに要求されるRF信号処理機能を部分的にでも明らかにし、これまでの成果を適用して、「集積化」技術を向上させるよう努力する。

謝辞

本研究を進めるにあたり、常に我がグループを支援して下さった葉原会長、古濱社長に深謝します。また、研究目標について熱心に討議し鼓舞して下さった前相川室長、田中主幹研究員に深謝します。学会での活躍の場を積極的に作って下さった赤池室長に深謝します。さらに、グループの研究員の方々には、研究推進に不可欠な設計·試作·評価や研究設備の整備において多大な協力を頂きました。心から感謝します。原研究員は受動回路の能動化を積極的に進め、LUFET MMIC研

究の一翼を担いました。また、その明るい性格はグループにとって不可欠な要素でした。中本研究員はプロセス･材料に関する経験･知識をグループに注入し、多層化MMICおよびデバイスモデルの研究に貢献しました。平岡研究員は手間のかかるデバイスシミュレータを継続して担当し、かつ、非線形回路MMIC･多層化MMICに成果を出しました。竹中研究技術員はMMIC測定･パタン作成等試作全般にわたって貢献し、かつ、ミキサを一貫して担当して頂きました。新しい概念を実りあるものにするために時には無理を言ったと思いますが、御容赦願います。研究所のその他の方々にも日ごろ、個人的かつ仕事上で大変お世話になりましたことを感謝します。特に、高橋課長には事務手続き上で、また個人的に御迷惑をおかけしました。角田研究員には電磁界解析について御教授頂きました。また、電解横モード有限要素法(豊田研修研究員(阪大)作成)についてプリプロセッサを作成し、だれでも使い易いソフトウェアにして頂きました。Davis氏には英文論文のチェックや議論を快く行って頂きました。

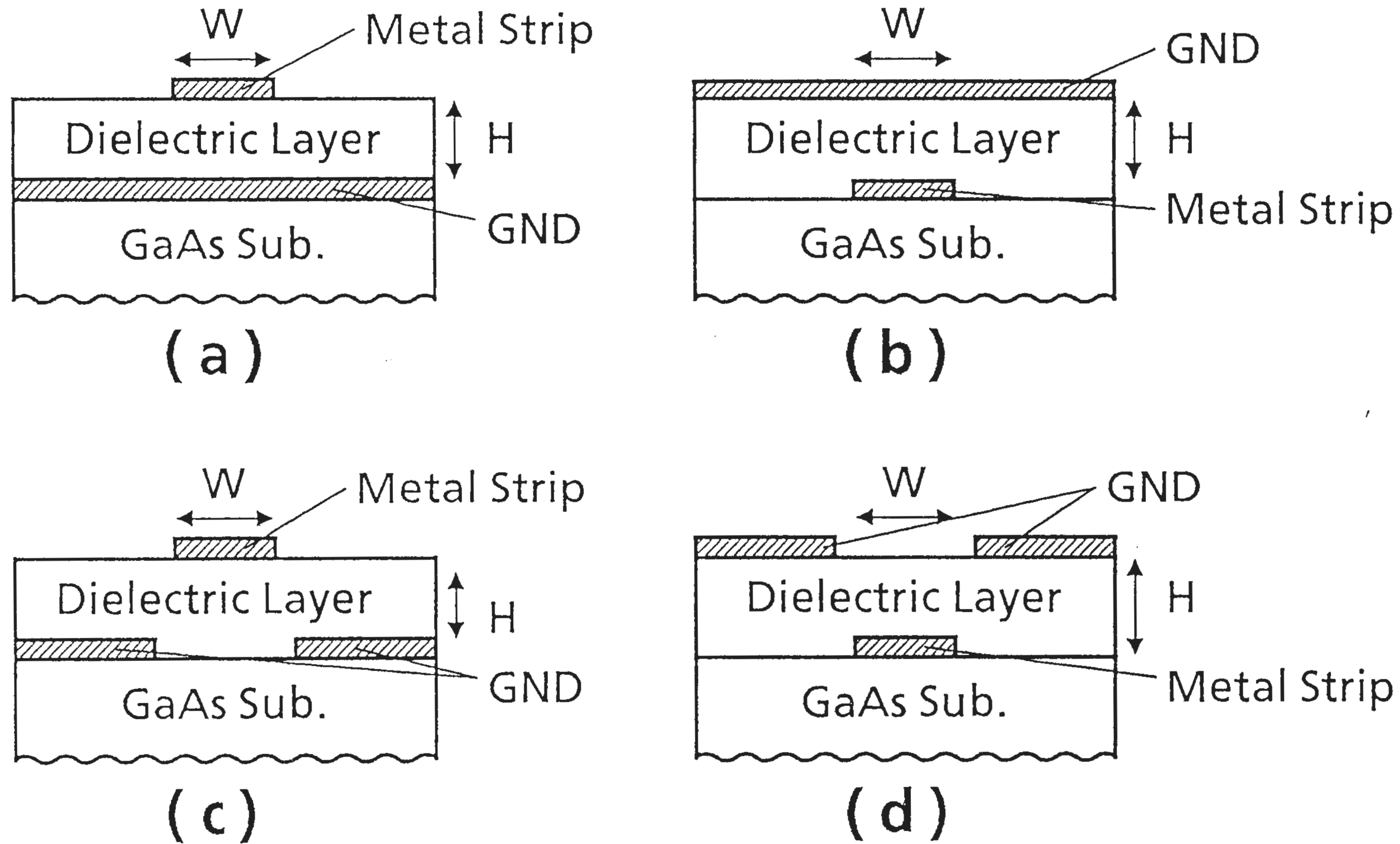
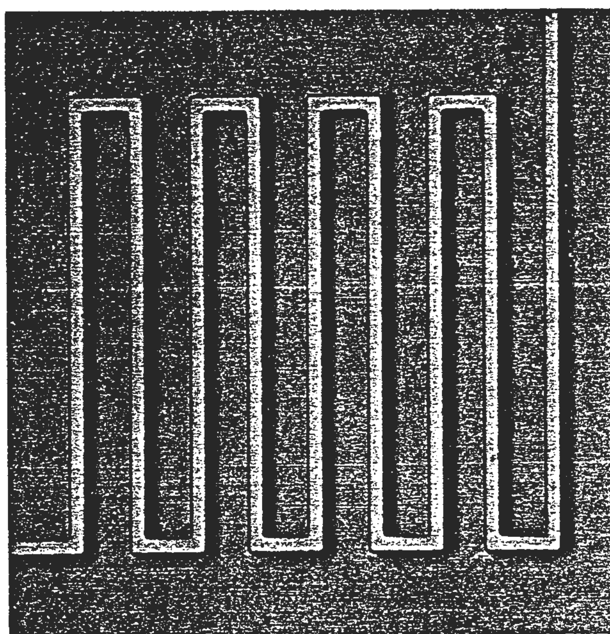


Fig. 3.1. Examples of miniature transmission lines fabricated using a thin dielectric film. (a) is a thin film microstrip (TFMS) line, (b) inverted TFMS line, and (c) and (d) quasi-coplanar waveguide.



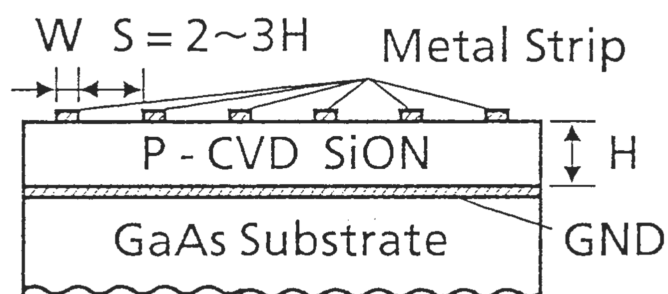
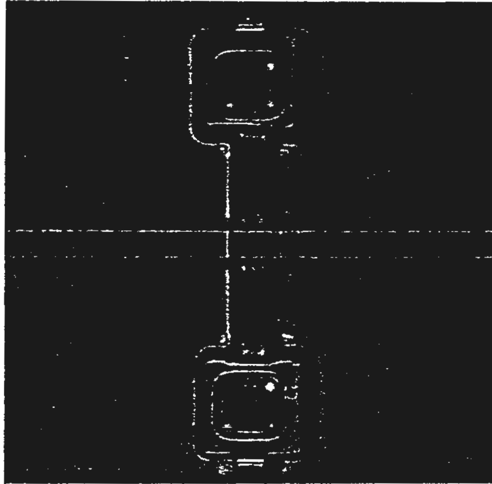


Fig. 3.2. A meander-like TFMS line. (a) Top view. (b) Cross-sectional view.



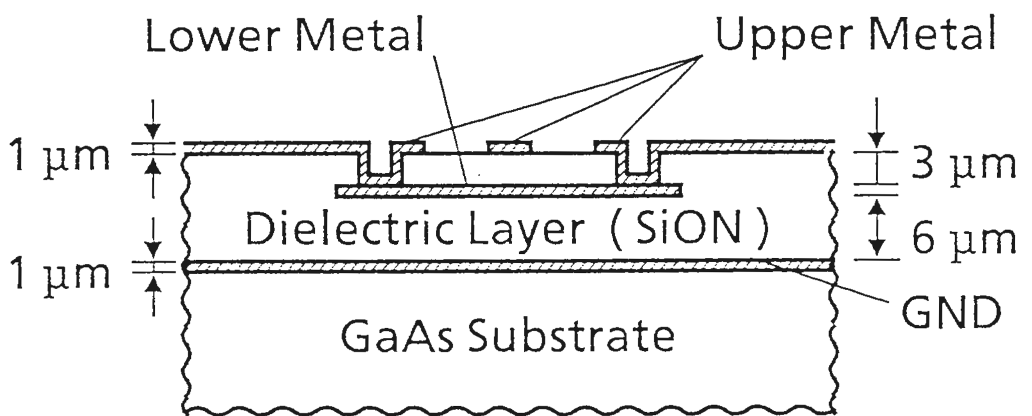


Fig. 3.3. A TFMS line crossover. (a) Top view. (b) Cross-sectional view.

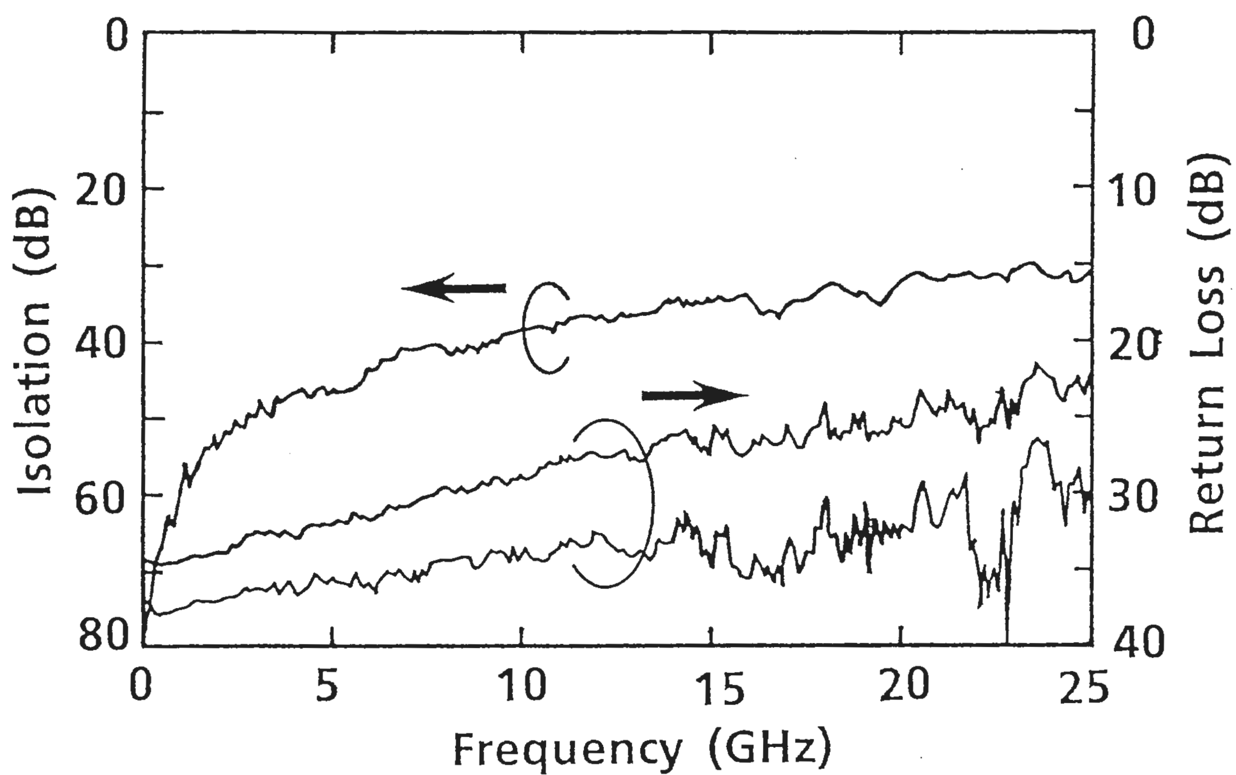
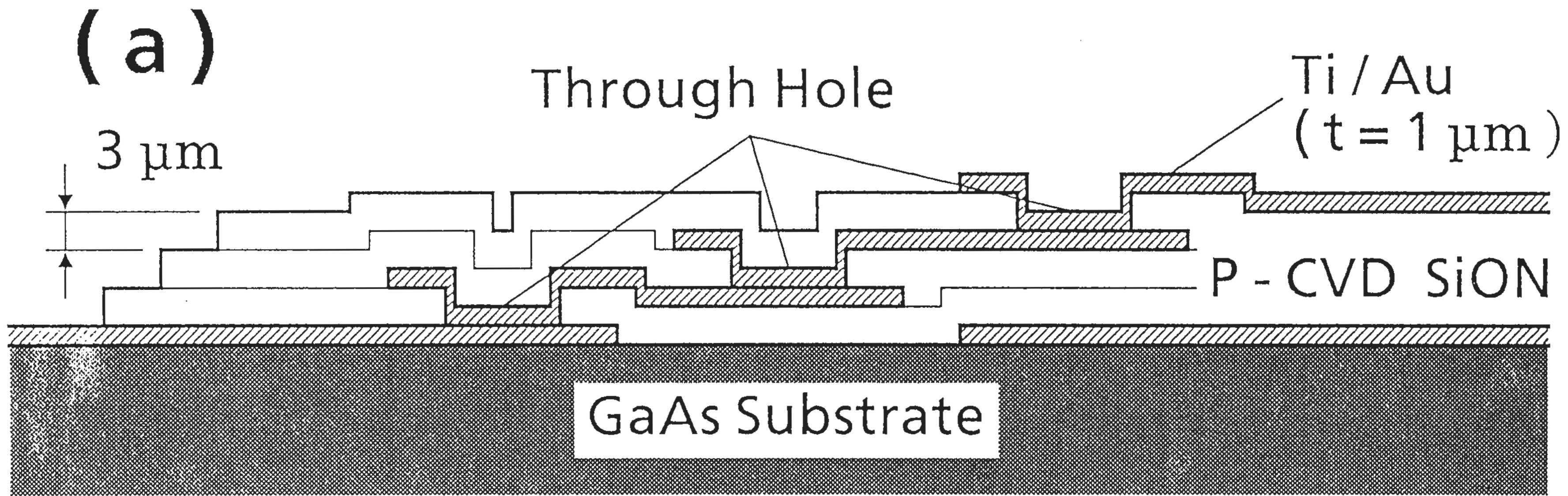


Fig. 3.4. Measured characteristics of a 50Ω TFMS line crossover.



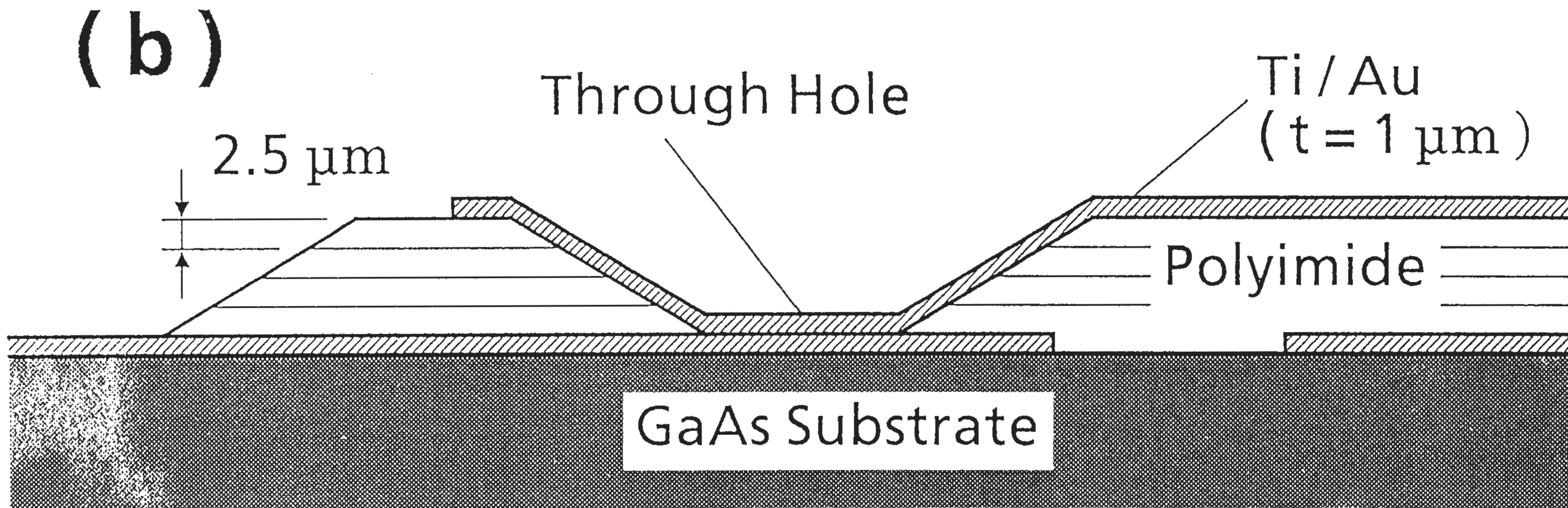


Fig. 3.5. Vertical connections through (a) SiON and (b) polyimide layers.

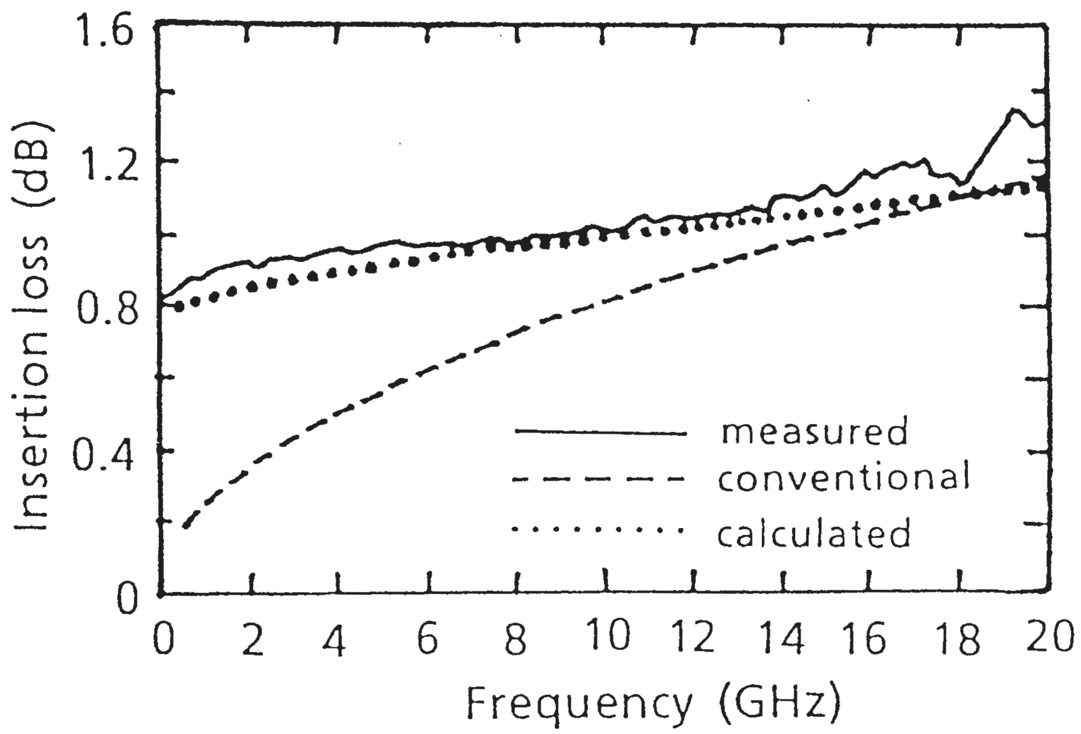


Fig. 3.6. TFMS experiment and calculated results.

● measured

10

1

0.1

0.01

Loss (dB/mm)

$Z_0 = 50\Omega$

w

t

H

GaAs sub.

t

w

t

GaAs sub.

H

GaAs (t = 3μm)

f = 20GHz

f = 10GHz

f ≐ 2GHz

SiON

(t = H/3μm)

1 10 100 1000

H (μm)

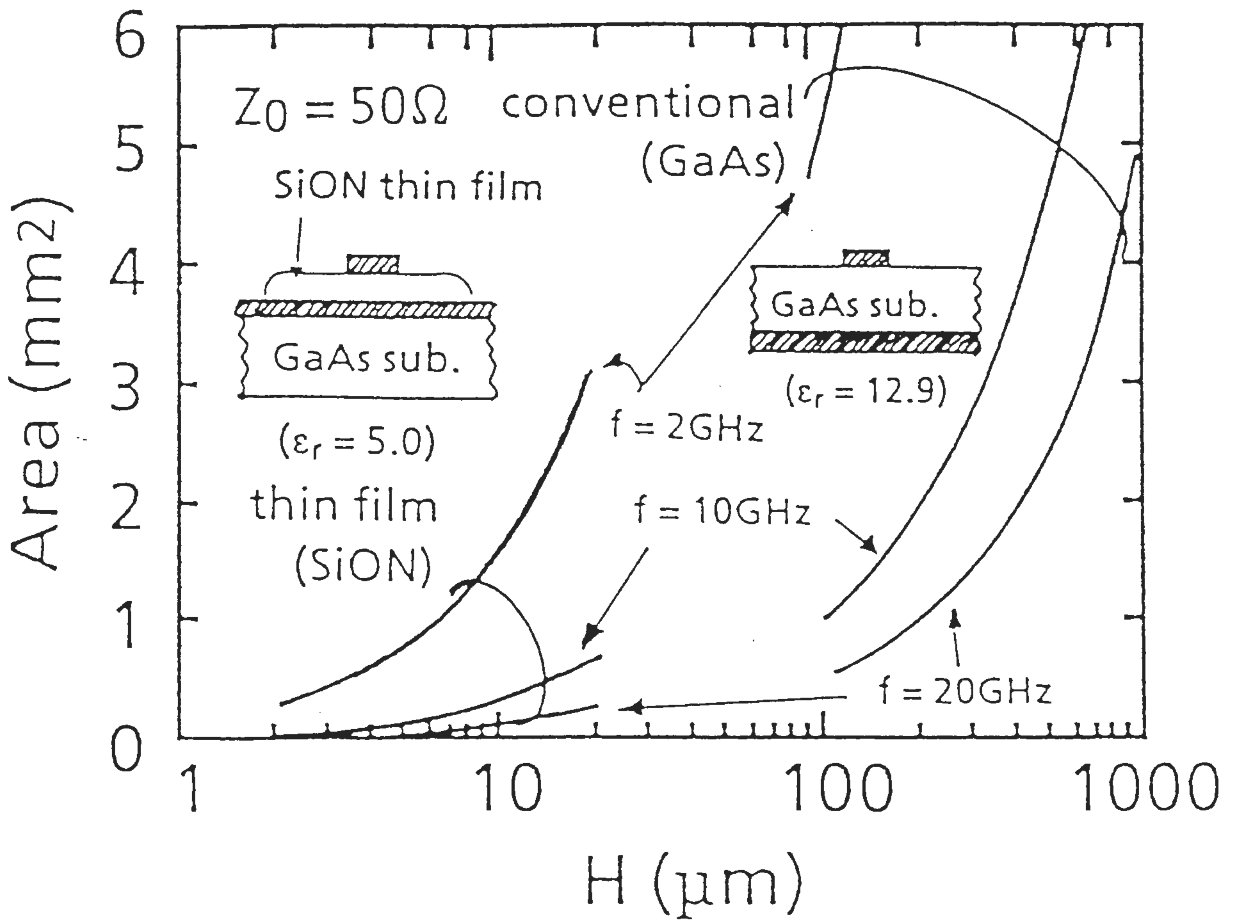


Fig. 3.7. Characteristics of TFMS and conventional microstrip lines.

Fig. 3.8. Chip area of TFMS and conventional microstrip lines.

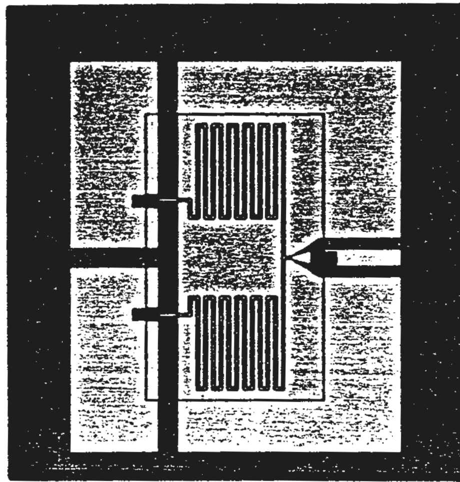
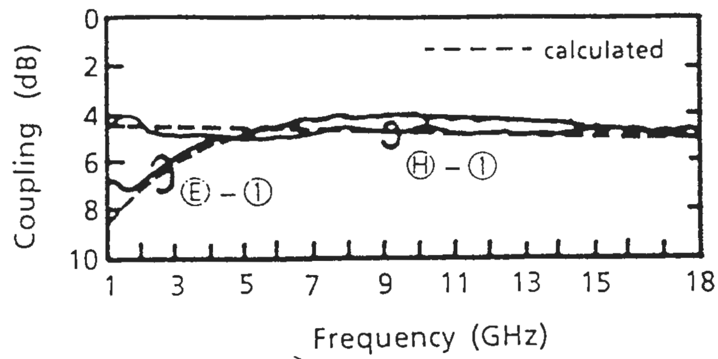
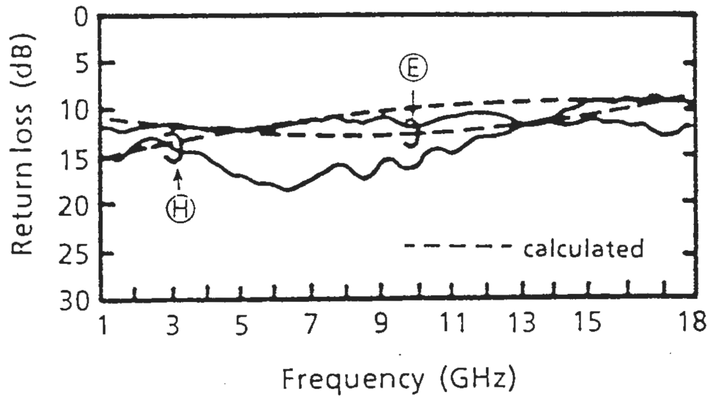
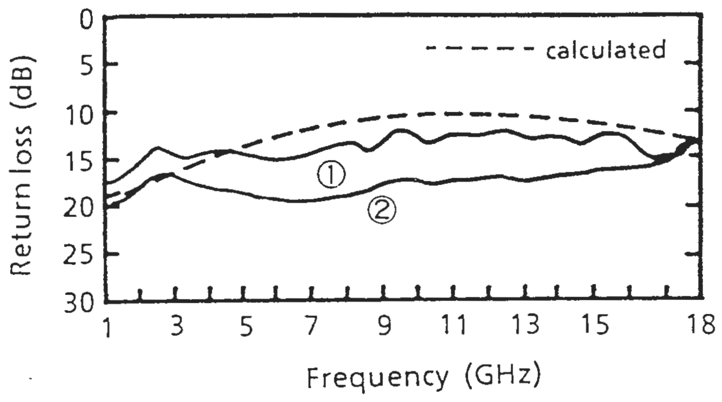


Fig. 3.9. Photomicrograph of a fabricated MMIC magic T.







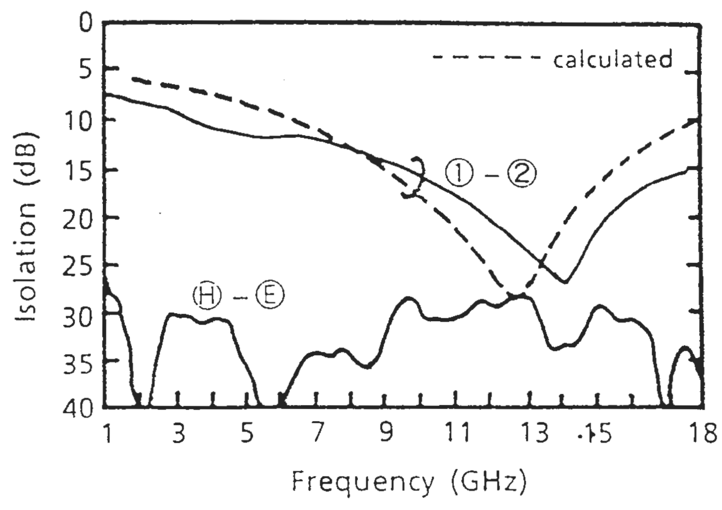


Fig. 3.10. Measured and calculated performance of the magic T. (a) Coupling between ports Ⓔ - ①, ②, and Ⓗ - ①, ②. (b) Return loss at ports Ⓔ and Ⓗ. (c) Return loss at ports ① and ②. (d) Isolation between ports ① - ② and Ⓔ - Ⓗ.

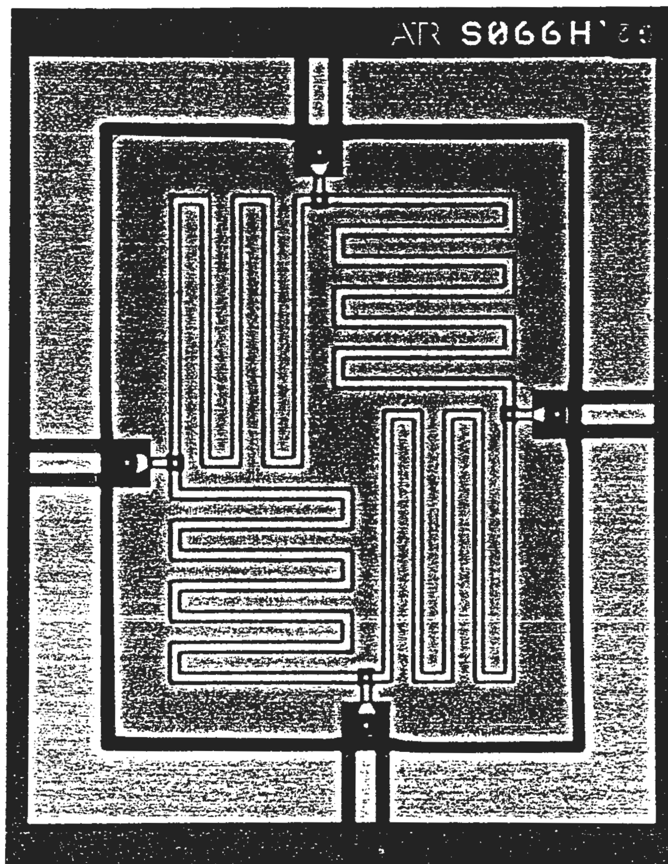
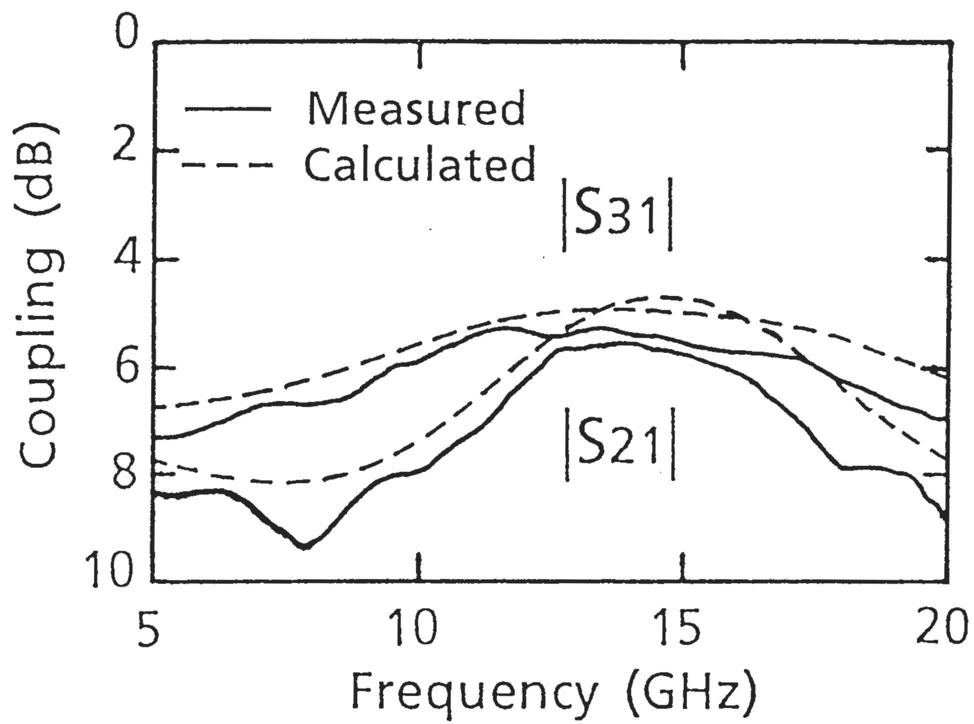


Fig. 3.11. Photomicrograph of a 15GHz branch-line coupler using TFMS lines on two different layers.



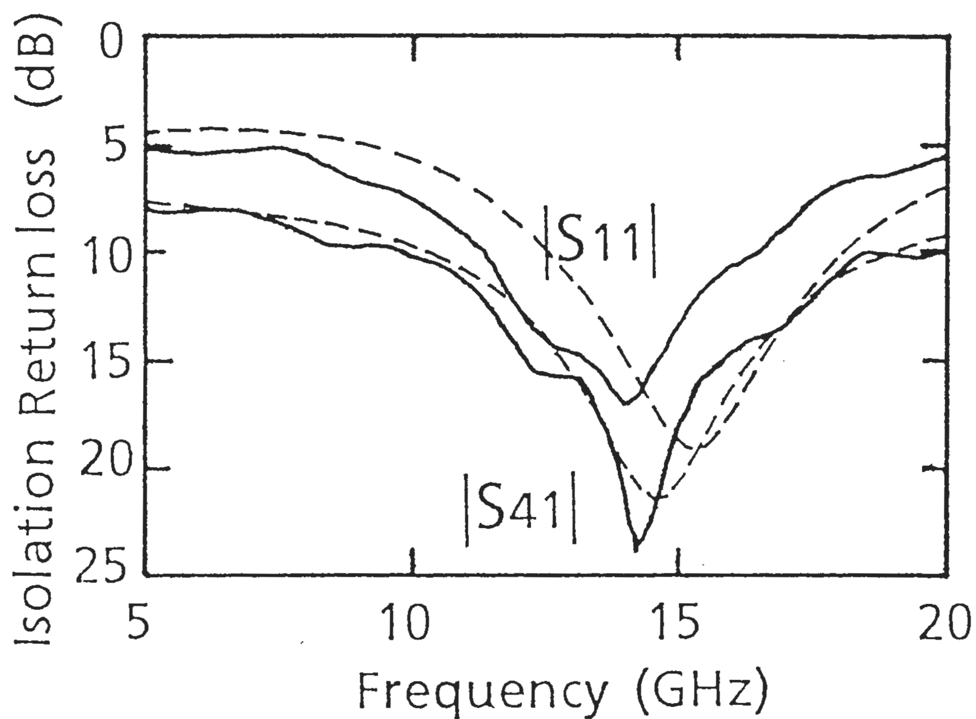


Fig. 3.12. Measured and calculated performance of the branch-line coupler MMIC.

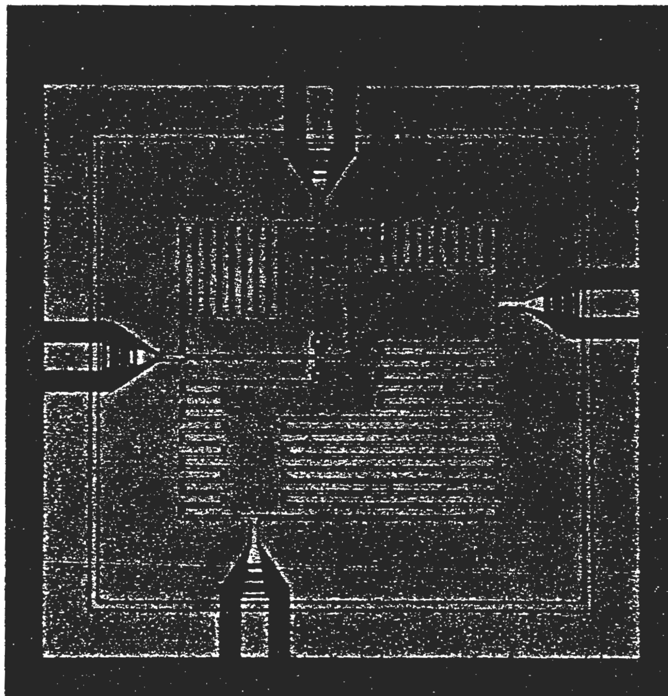
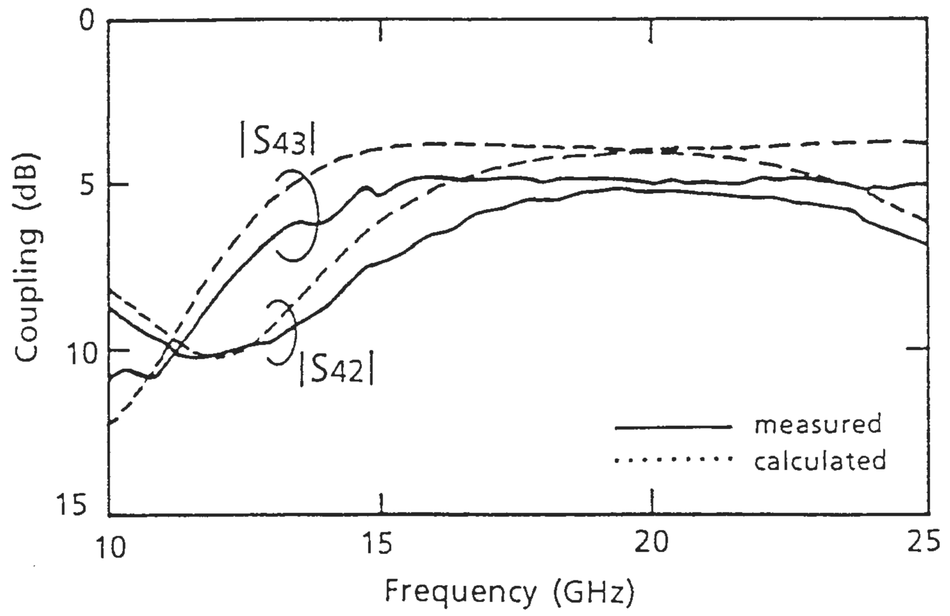
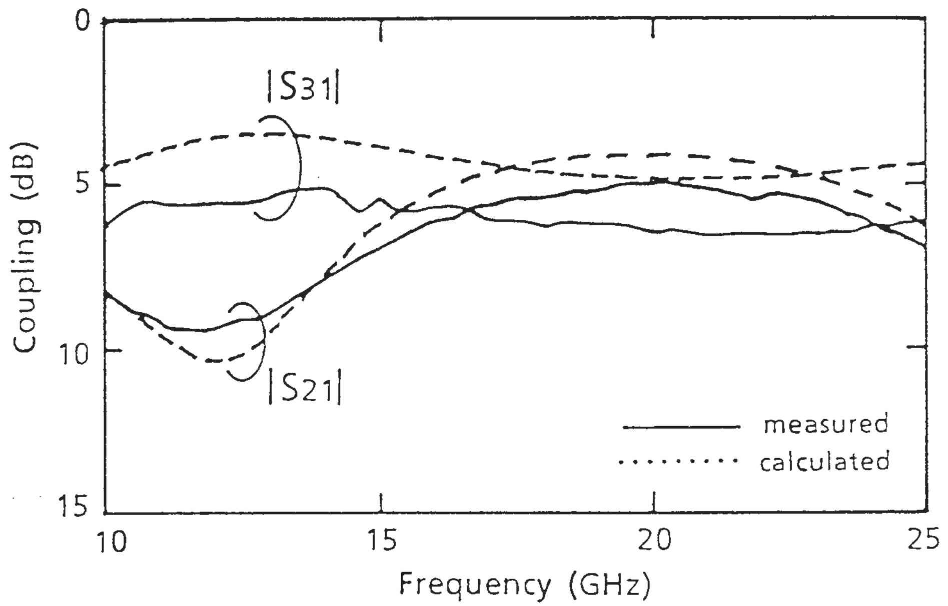


Fig. 3.13. Photomicrograph of a 20GHz port-interchanged rat-race hybrid using a line crossover.



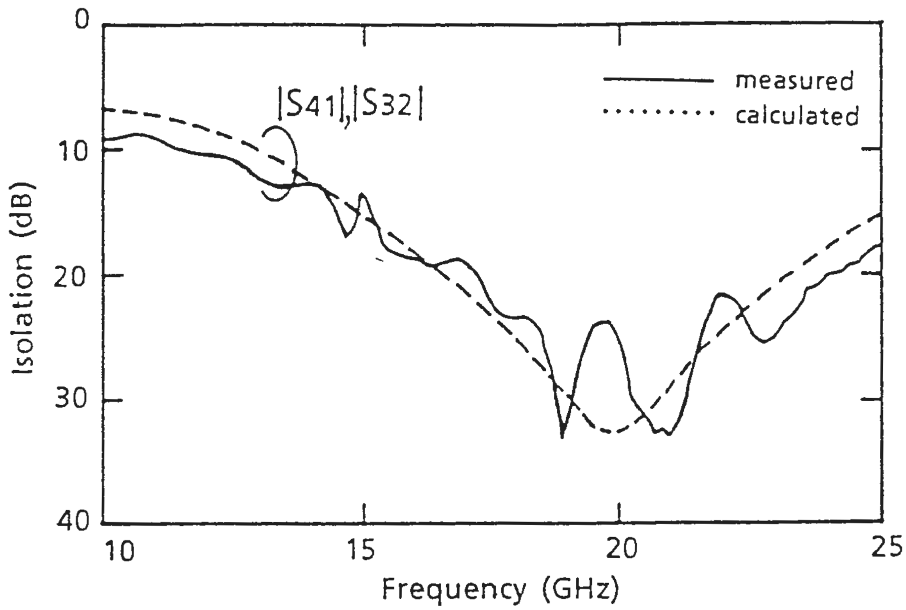
Coupling ④ - ②, ③



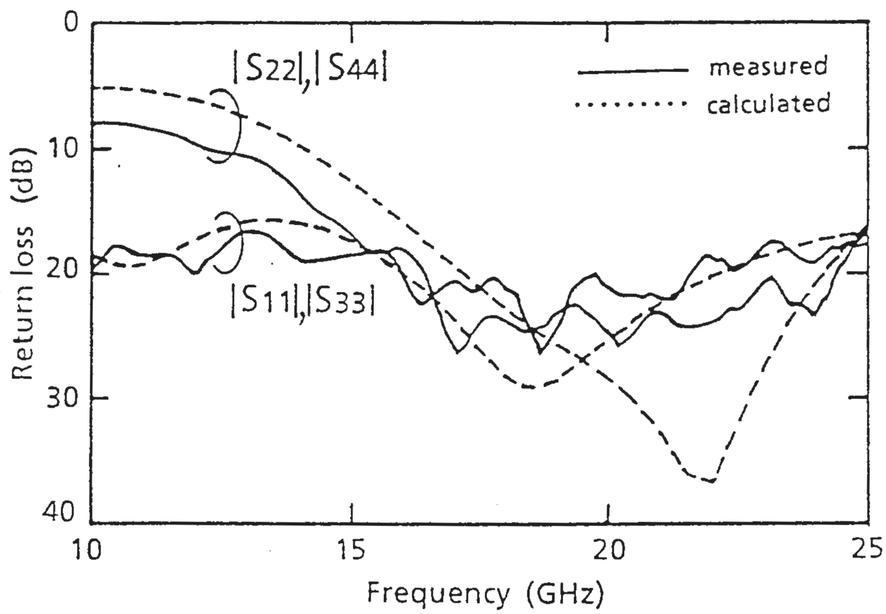
Coupling ① - ②, ③

Measured performance

Fig. 3.14. Measured and calculated performance of the port-interchanged rat-race hybrid MMIC.



Isolation ④ - ①, ③ - ②



Return loss ①, ②, ③, ④

Measured performance.

Fig. 3.14. Measured and calculated performance of the port-interchanged rat-race hybrid MMIC.

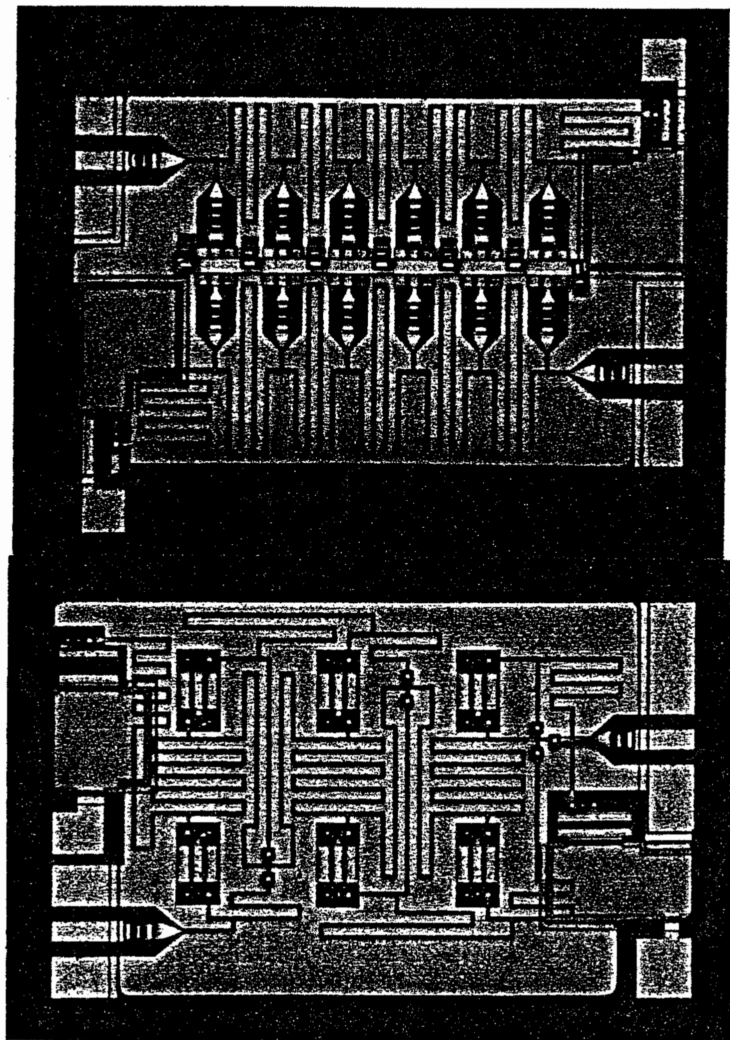


Fig. 3.15. Photomicrographs of 6-stage distributed amplifier MMICs with the same equivalent circuit scheme and parameters.

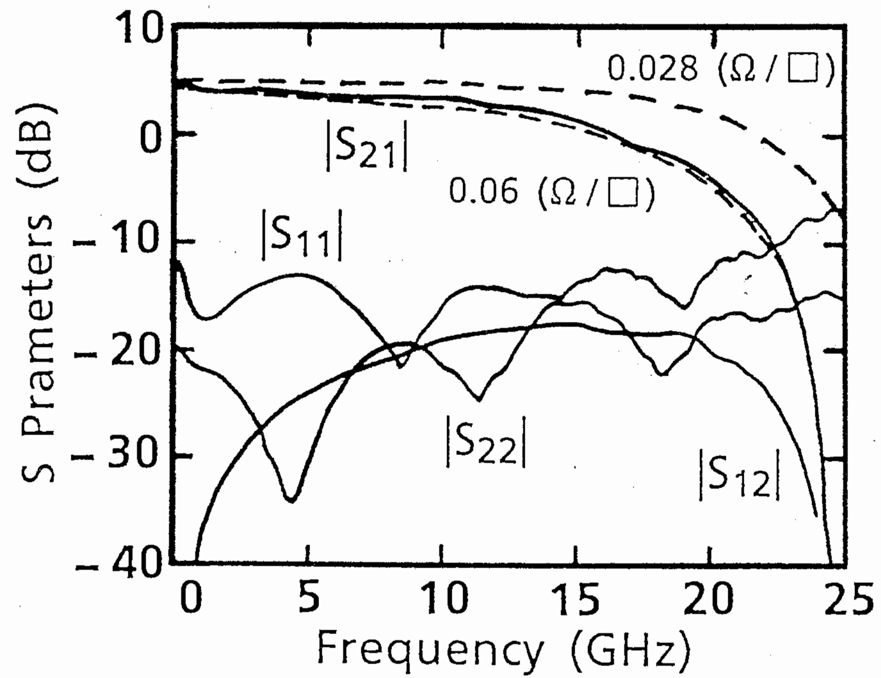


Fig. 3.16. Performance of the distributed amplifier MMICs. Solid: measured, dash: calculated.

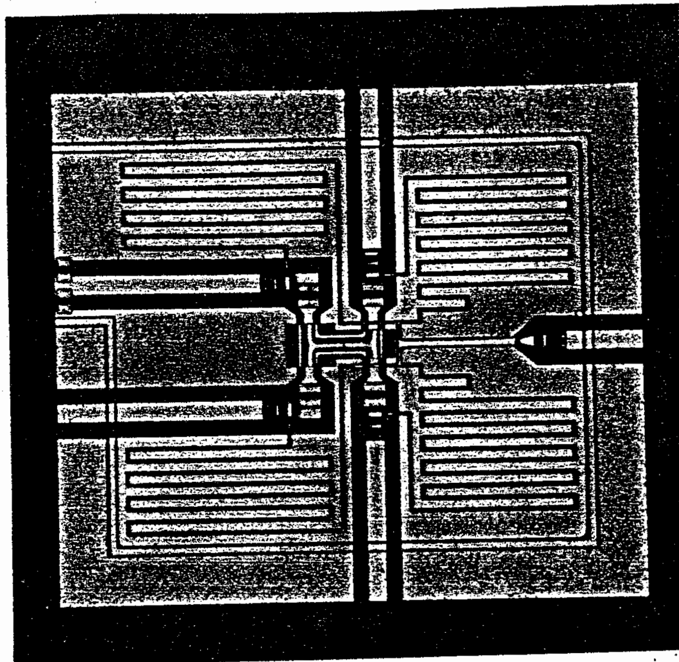


Fig. 3.17. Photomicrograph of a 12-GHz, 4-port Wilkinson divider using vertical connections.

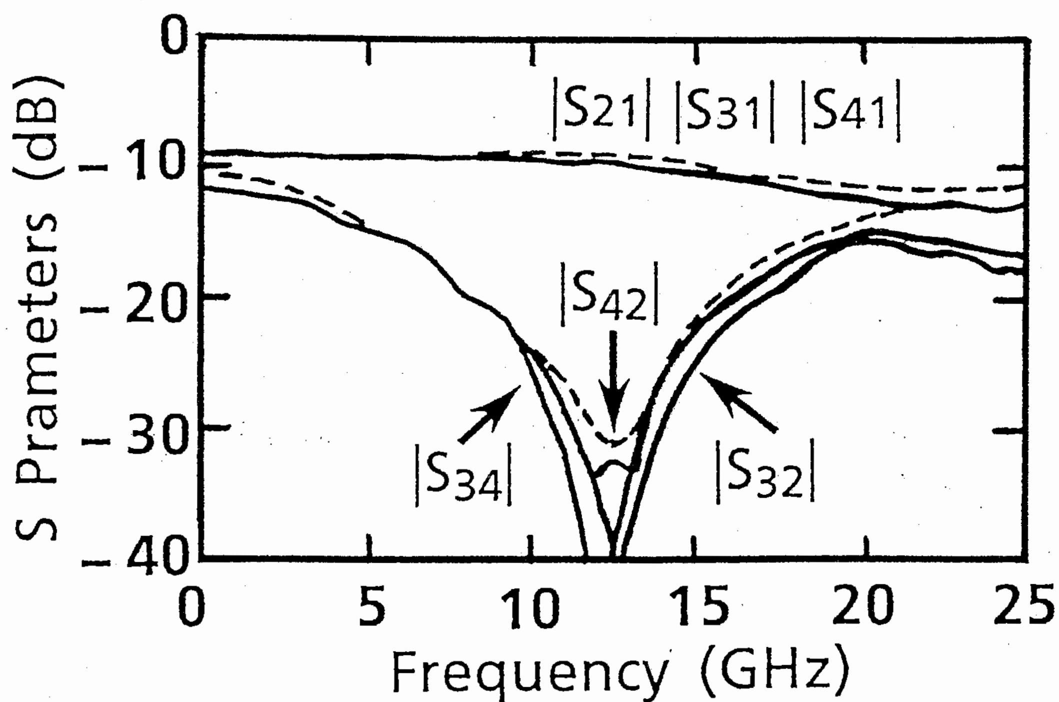


Fig. 3.18. Isolation and power dividing characteristics of the 4-port Wilkinson divider. Solid: measured, dash: calculated (R_{s0}=0.06 Ω/□).